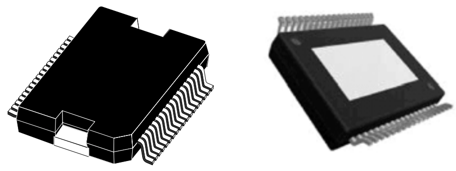
L9954
L9954XP

Door actuator driver

Features

- Three half bridges for 1.5A load (R_{on}=800mΩ)
- One highside driver for 6A load (R_{on}=100mΩ)
- Two highside drivers for 1.5A load (R_{on}=800mΩ)
- Programmable softstart function to drive loads with higher inrush currents (i.e. current >6A, >1.5A)
- Very low current consumption in standby mode (I_S < 6µA typ; $T_j \leq$ 85 °C)
- All outputs short circuit protected
- Current monitor output for highside OUT1, OUT4, OUT5 and OUT6
- All outputs over temperature protected
- Open load diagnostic for all outputs
- Overload diagnostic for all outputs
- PWM control of all outputs
- Charge pump output for reverse polarity protection



PowerSO-36 PowerSSO-36

Applications

- Door actuator driver with bridges for mirror axis control and highside driver for mirror defroster and two 10W-light bulbs.

Description

The L9954 and L9954XP are microcontroller driven, multifunctional door actuator drivers for automotive applications. Up to two DC motors and three grounded resistive loads can be driven with three half bridges and three highside drivers. The integrated standard serial peripheral interface (SPI) controls all operation modes (forward, reverse, brake and high impedance). All diagnostic information is available via the SPI.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-36	L9954	L9954TR
PowerSSO-36	L9954XP	L9954XPTR

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

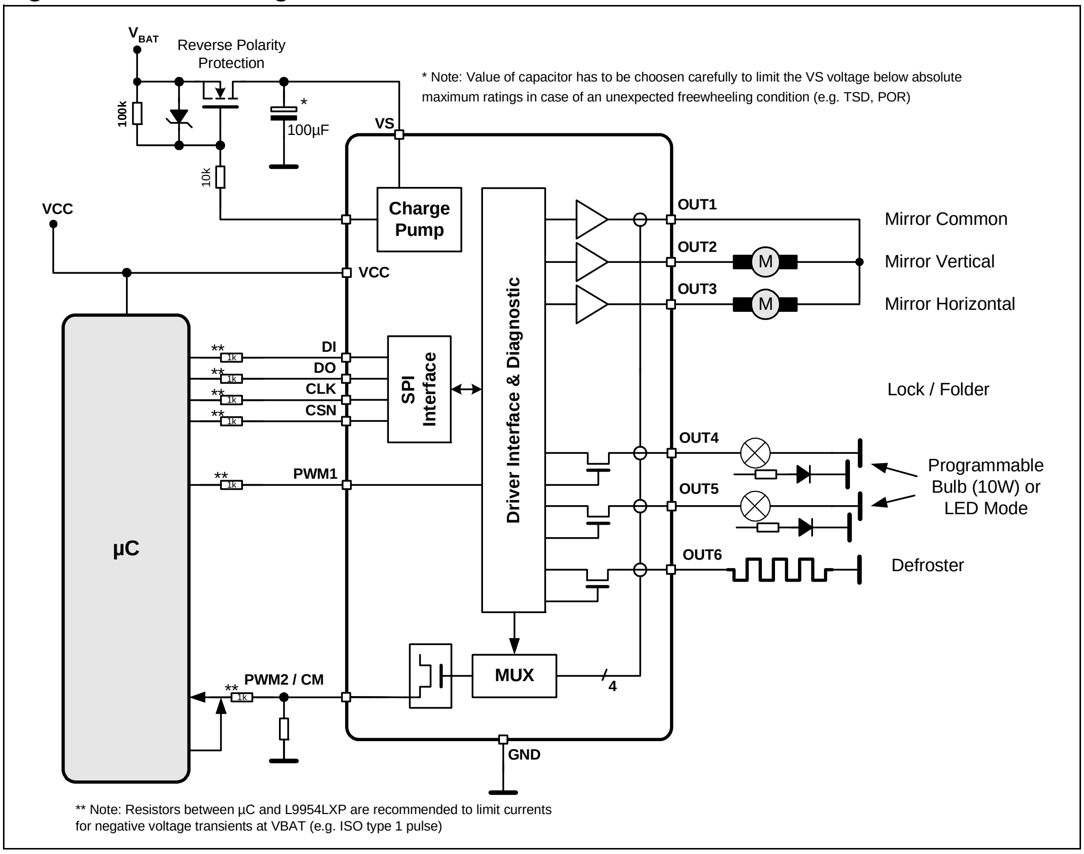


Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground : Reference potential Important: for the capability of driving the full current at the outputs all pins of GND must be externally connected.
2, 35	OUT6	Highside-driver-output 6 The output is built by a highside switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The highside driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current and open load protected. Important: for the capability of driving the full current at the outputs both pins of OUT6 must be externally connected.

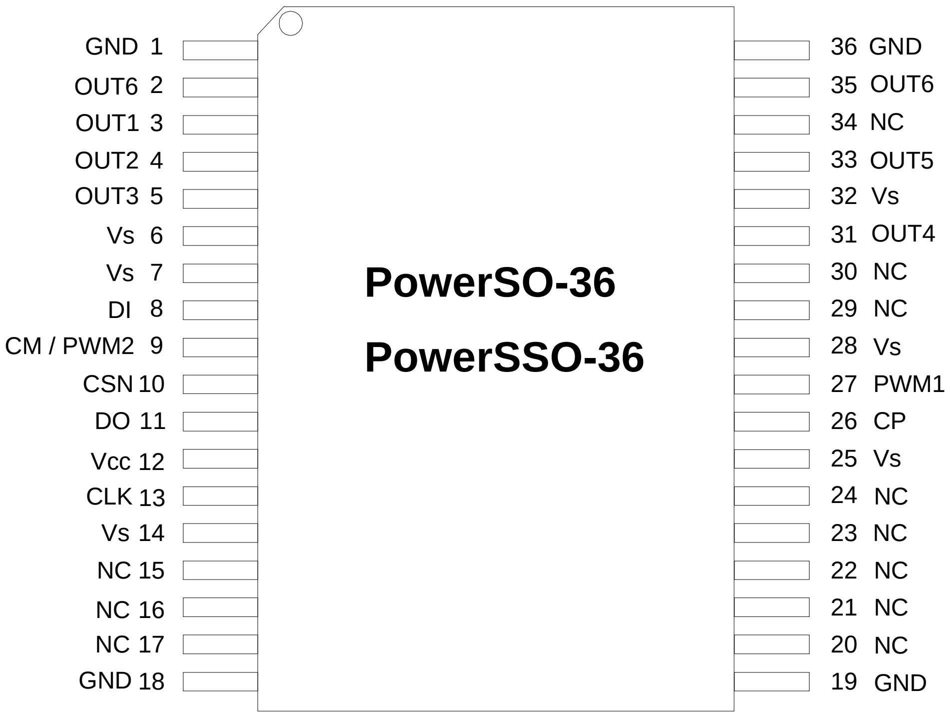
Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
3 4 5	OUT1 OUT2 OUT3	Half-bridge-output 1,2,3 The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: highside driver from output to VS, lowside driver from GND to output). This output is over-current and open load protected.
6, 7, 14, 25, 28, 32	V_S	Power supply voltage (external reverse protection required) For this input a ceramic capacitor as close as possible to GND is recommended. Important: for the capability of driving the full current at the outputs all pins of VS must be externally connected.
8	DI	Serial data input The input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 24bit control word and the least significant bit (LSB, bit 0) is transferred first.
9	CM/PWM2	Current monitor output/PWM2 input Depending on the selected multiplexer bits of Input Data Register this output sources an image of the instant current through the corresponding highside driver with a ratio of 1/10.000. This pin is bidirectional. The microcontroller can overdrive the current monitor signal to provide a second PWM input for the output OUT5.
10	CSN	Chip select not input / testmode This input is low active and requires CMOS logic levels. The serial data transfer between L9954 and micro controller is enabled by pulling the input CSN to low level.
11	DO	Serial data output The diagnosis data is available via the SPI and this tristate-output. The output will remain in tristate, if the chip is not selected by the input CSN (CSN = high)
12	V_{CC}	Logic supply voltage For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input This input controls the internal shift register of the SPI and requires CMOS logic levels.
26	CP	Charge pump output This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection.
27	PWM1	PWM1 input This input signal can be used to control the drivers OUT1-OUT4 and OUT6 by an external PWM signal.

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
31 33	OUT4, OUT5	Highside-driver-output 4 and 5 Each output is built by a highside switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. Each highside driver is a power DMOS transistor with an internal parasitic reverse diode from each output to VS (bulk-drain-diode). Each output is over-current and open load protected.
15, 16, 17, 20, 21, 22, 23, 24, 29, 30, 34	NC	Not connected pins.

Figure 2. Configuration diagram (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to28	V
	Single pulse t_{max} < 400ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI}, V_{DO}, V_{CLK}, V_{CSN}, V_{pwm1}	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{CM}	Current monitor output	-0.3 to V_{CC} + 0.3	V
V_{CP}	Charge pump output	-25 to V_S + 11	V
$I_{OUT1,2,3,4,5}$	Output current	±5	A
I_{OUT6}	Output current	±10	A

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	± 2 (1)	kV
Output pins: OUT1 - OUT6	± 8 (2)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.
2. HBM with all unzapped pins grounded.

2.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j	130		150	°C
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing			170	°C
$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	T_j decreasing	150			°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis			5		°K

2.4 Electrical characteristics

V_S = 8 to 16V, V_{CC} = 4.5 to 5.3V, T_j = - 40 to 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
V_S	Operating supply voltage range		7		28	V
I_S	V_S DC supply current	V_S = 16V, V_{CC} = 5.3V active mode OUT1 - OUT6 floating		7	20	mA
	V_S quiescent supply current	V_S = 16V, V_{CC} = 0V standby mode OUT1 - OUT6 floating T_{test} = -40°C, 25°C		4	12	µA
		T_{test} = 85°C (1)		6	25	µA
I_{CC}	V_{CC} DC supply current	V_S = 16V, V_{CC} = 5.3V CSN = V_{CC} , active mode		1	3	mA
	V_{CC} quiescent supply current	V_S = 16V, V_{CC} = 5.3V CSN = V_{CC} standby mode OUT1 - OUT6 floating		25	50	µA
$I_S + I_{CC}$	Sum quiescent supply current	V_S = 16V, V_{CC} = 5.3V CSN = V_{CC} standby mode OUT1 - OUT6 floating T_{test} = 130°C		50	100	µA

1. Guaranteed by design.

Table 8. Overvoltage and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
$V_{SUV\ ON}$	VS UV-threshold voltage	V_S increasing	5.7		7.2	V
$V_{SUV\ OFF}$	VS UV-threshold voltage	V_S decreasing	5.5		6.9	V
$V_{SUV\ hyst}$	VS UV-hysteresis	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$		0.5		V
$V_{SOV\ OFF}$	VS OV-threshold voltage	V_S increasing	18		24.5	V
$V_{SOV\ ON}$	VS OV-threshold voltage	V_S decreasing	17.5		23.5	V
$V_{SOV\ hyst}$	VS OV-hysteresis	$V_{SOV\ OFF}$ - $V_{SOV\ ON}$		1		V
$V_{POR\ OFF}$	Power-On-reset threshold	V_{CC} increasing			4.4	V
$V_{POR\ ON}$	Power-On-reset threshold	V_{CC} decreasing	3.1			V
$V_{POR\ hyst}$	Power-On-reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.3		V

Table 9. Current monitor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range	V_{CC} = 5V	0		4	V
$I_{CM,r}$	Current monitor output ratio: I_{CM} / $I_{OUT1,4,5,6}$	0V ≤ V_{CM} ≤ 4V, VCC=5V		$\frac{1}{10.000}$		-
$I_{CM\ acc}$	Current monitor accuracy	0 V ≤ V_{CM} ≤ 3.8V, V_{CC} = 5V, $I_{Out,min}$=500mA, $I_{Out\ max}$ = 6A (FS = full scale= 600µA)		4% + 1%FS	8% + 2%FS	-

Table 10. Charge pump output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 8V, I_{CP} = -60µA	V_S+6		V_S+13	V
		V_S = 10V, I_{CP} = -80µA	V_S+8		V_S+13	V
		V_S ≥ 12V, I_{CP} = -100µA	V_S+10		V_S+13	V
I_{CP}	Charge pump output current	V_{CP} = V_S+10V, V_S =13.5V	95	150	300	µA

Table 11. OUT1 - OUT6

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT1}$, $r_{ON\ OUT2}$ $r_{ON\ OUT3}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT1,2,3}$ = ± 0.8A		800	1100	mΩ
		V_S = 13.5 V, T_j = 125 °C, $I_{OUT1,2,3}$ = ± 0.8 A		1250	1700	mΩ
$r_{ON\ OUT4}$, $r_{ON\ OUT5}$	On-resistance to supply	V_S = 13.5 V, T_j = 25 °C, $I_{OUT4,5}$ = –0.8 A		500	700	mΩ
		V_S = 13.5 V, T_j = 125 °C, $I_{OUT4,5}$ = –0.8 A		700	950	mΩ
$r_{ON\ OUT6}$	On-resistance to supply	VS = 13.5 V, T_j = 25 °C, I_{OUT6} = – 3 A		100	150	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT6} = –3 A		150	200	mΩ
I_{OUT1} I_{OUT2} I_{OUT3}	Output current limitation to GND	Source, V_S=13.5 V	-3.0		-1.5	A
I_{OUT1} I_{OUT2} I_{OUT3}	Output current limitation to supply	Sink, V_S=13.5 V	1.5		3.0	A
I_{OUT4} I_{OUT5}	Output current limitation to GND	Source, V_S=13.5 V	-3.0		-1.5	A
I_{OUT6}	Output current limitation to GND	Source, V_S=13.5 V	-10.5		-6	A
$t_{d\ ON\ H}$	Output delay time, highside driver On	V_S=13.5 V, corresponding lowside driver is not active	20	40	80	µs
$t_{d\ OFF\ H}$	Output delay time, highside driver Off	V_S=13.5 V	50	150	300	µs
$t_{d\ ON\ L}$	Output delay time, lowside driver On	V_S=13.5 V, corresponding highside driver is not active	15	30	70	µs
$t_{d\ OFF\ L}$	Output delay time, lowside driver Off	V_S=13.5 V	80	150	300	µs
$t_{d\ HL}$	Cross current protection time, source to sink	$t_{CC\ ONLS\_OFFHS}$ - $t_{d\ OFF\ H}$ (1)		200	400	µs
$t_{d\ LH}$	Cross current protection time, sink to source	$t_{CC\ ONHS\_OFFLS}$ - $t_{d\ OFF\ L}$ (1)		200	400	µs
I_{QLH}	Switched-off output current highside drivers of OUT1-6	V_{OUT1-6}= 0V, standby mode	0	-2	-5	µA
		V_{OUT1-6}= 0V, active mode	-40	-15	0	µA

Table 11. OUT1 - OUT6 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{QLL}	Switched-off output current lowside drivers of OUT1-3	$V_{OUT1-3}= V_S$, standby mode	0	80	120	µA
		$V_{OUT1-3}= V_S$, active mode	-40	-15	0	µA
I_{OLD123}	Open load detection current of OUT1, OUT2 and OUT3	Source and sink	15	40	60	mA
I_{OLD45}	Open load detection current of OUT4 and OUT5	Source and sink	15	40	60	mA
I_{OLD6}	Open load detection current of OUT6	Source	30	150	300	mA
$t_{d\ OL}$	Minimum duration of open load condition to set the status bit		500		3000	µs
t_{ISC}	Minimum duration of over-current condition to switch off the driver		10		100	µs
f_{rec0}	Recovery frequency for OC recovery duty cycle bit=0		1		4	kHz
f_{rec1}	Recovery frequency for OC recovery duty cycle bit=1		2		6	kHz
dV_{OUT123}/dt dV_{OUT45}/dt	Slew rate of OUT_{123} and OUT_{45}	V_S =13.5 V R_{load} = 16.8 Ω	0.08	0.2	0.4	V/µs
dV_{OUT6}/dt	Slew rate of OUT_6	V_S =13.5 V R_{load} = 4.5 Ω	0.08	0.2	0.4	V/µs

1. $t_{CC\ ON}$ is the switch on delay time $t_{d\ ON}$ if complement in half bridge has to switch Off.

2.5 SPI - electrical characteristics

(V_S = 8 to 16V, V_{CC} = 4.5 to 5.3V, T_j = - 40 to 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin).

Table 12. Delay time from standby to active mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Delay time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	µs

Table 13. Inputs: CSN, CLK, PWM1/2 and DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{inL}	Input low level	V_{CC} = 5V	1.5	2.0		V
V_{inH}	Input high level	V_{CC} = 5V		3.0	3.5	V
V_{inHyst}	Input hysteresis	V_{CC} = 5V	0.5			V
$I_{CSN\ in}$	Pull up current at input CSN	V_{CSN} = 3.5V V_{CC} = 5V	-40	-20	-5	µA
$I_{CLK\ in}$	Pull down current at input CLK	V_{CLK} = 1.5V	10	25	50	µA
$I_{DI\ in}$	Pull down current at input DI	V_{DI} = 1.5V	10	25	50	µA
$I_{PWM1\ in}$	Pull down current at input PWM1	V_{PWM} = 1.5V	10	25	50	µA
C_{in}(1)	Input capacitance at input CSN, CLK, DI and PWM1/2	0 V < V_{CC} < 5.3V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 14. DI timing (1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	V_{CC} = 5V	1000			ns
t_{CLKH}	Clock high time	V_{CC} = 5V	400			ns
t_{CLKL}	Clock low time	V_{CC} = 5V	400			ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_{CC} = 5V	400			ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_{CC} = 5V	400			ns
$t_{set\ DI}$	DI setup time	V_{CC} = 5V	200			ns
$t_{hold\ DI}$	DI hold time	V_{CC} = 5V	200			ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_{CC} = 5V			100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_{CC} = 5V			100	ns

1. DI timing parameters tested in production by a passed / failed test:

Tj= -40°C / +25°C: SPI communication @ 2MHz.

Tj= +125°C SPI communication @ 1.25 MHz.

Table 15. DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	VCC = 5 V, I_D = -2mA		0.2	0.4	V
V_{DOH}	Output high level	VCC = 5 V, I_D = 2 mA	V_{CC} -0.4	V_{CC}-0.2		V

Table 15. DO (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DOLK}	Tristate leakage current	$V_{CSN} = V_{CC}$, $0V < V_{DO} < V_{CC}$	-10		10	µA
C_{DO} (1)	Tristate input capacitance	$V_{CSN} = V_{CC}$, $0V < V_{CC} < 5.3V$		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 16. DO timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{load} = -1mA		80	140	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{load} = 1mA		50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_L = 100 pF, I_{load} = 1mA pull-up load to V_{CC}		100	250	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_L = 100 pF, I_{load} = 4 mA pull-up load to V_{CC}		380	450	ns
$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_L =100 pF, I_{load} = -1mA pull-down load to GND		100	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_L = 100 pF, I_{load} = -4mA pull-down load to GND		380	450	ns
$t_{d\ DO}$	DO delay time	$V_{DO} < 0.3\ V_{CC}$, $V_{DO} > 0.7V_{CC}$, C_L = 100pF		50	250	ns

Table 17. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN\_HI,stb}$	CSN HI time, switching from standby mode	Transfer of SPI-command to Input Register	20			µs
$t_{CSN\_HI,min}$	CSN HI time, active mode	Transfer of SPI-command to input register	4			µs

Figure 3. SPI - transfer timing diagram

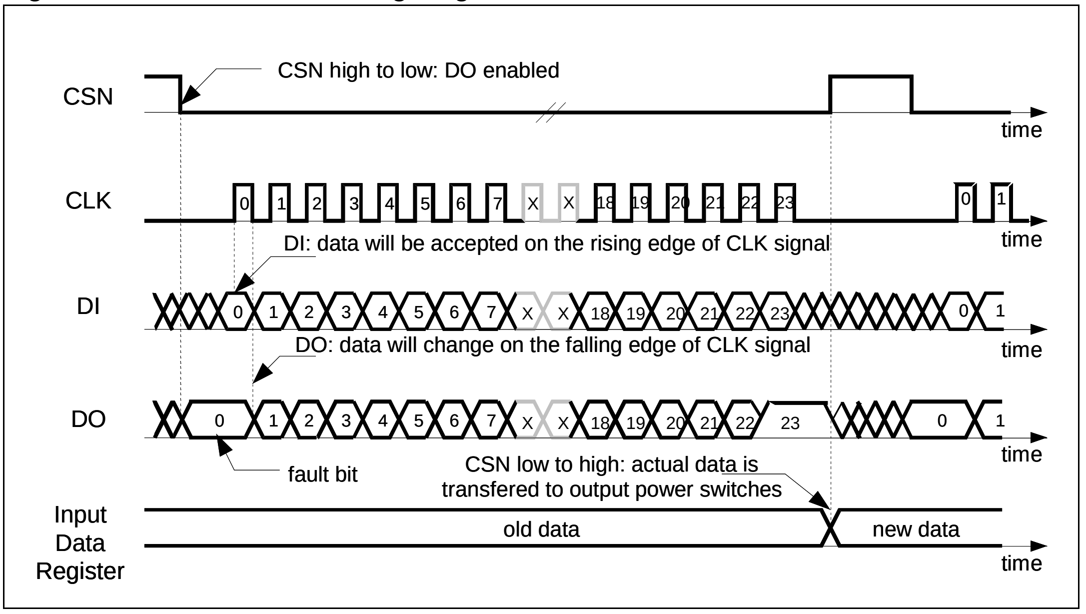


Figure 4. SPI - input timing

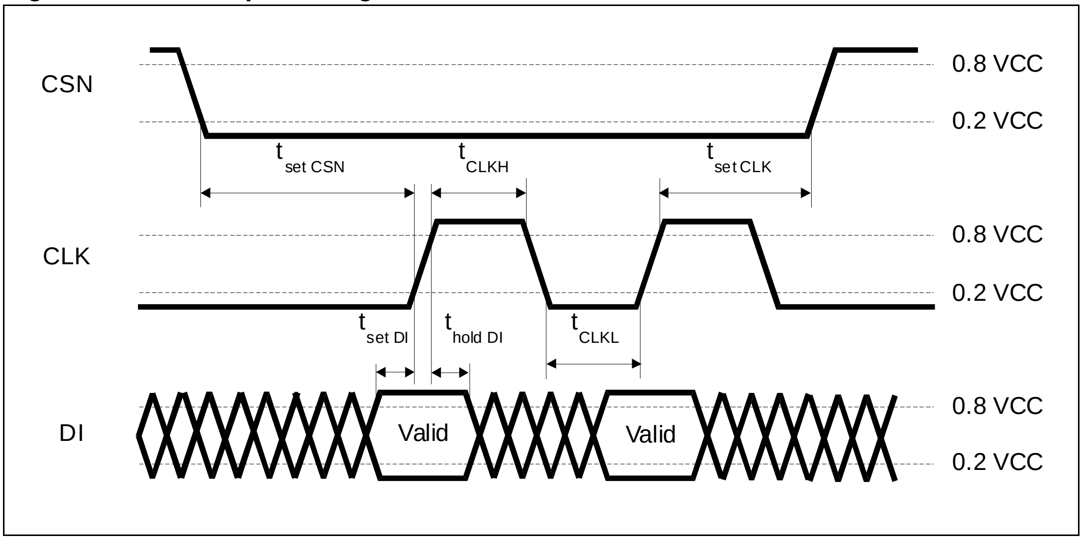


Figure 5. SPI - DO valid data delay time and valid time

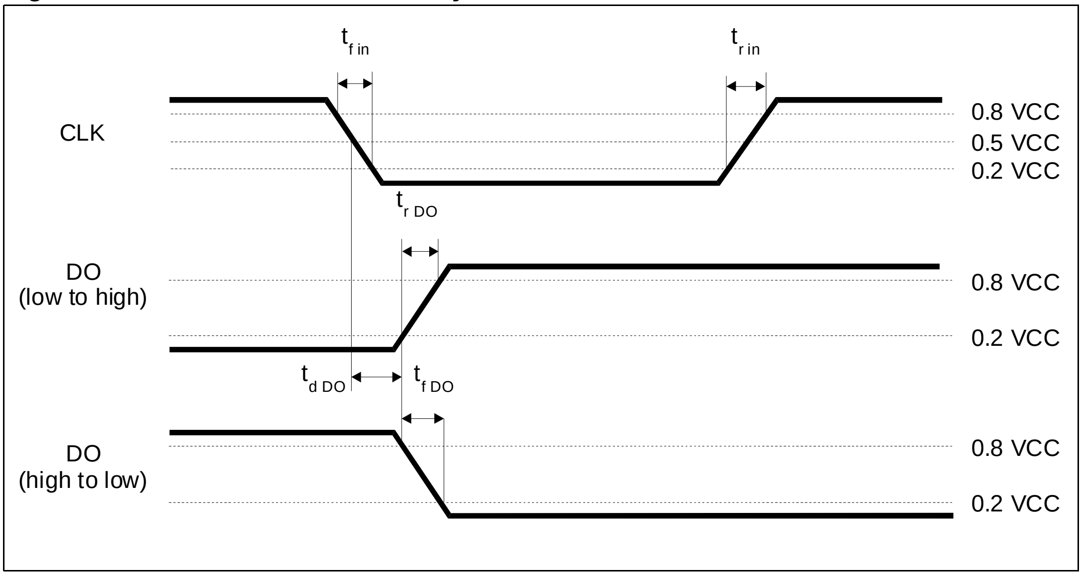


Figure 6. SPI - DO enable and disable time

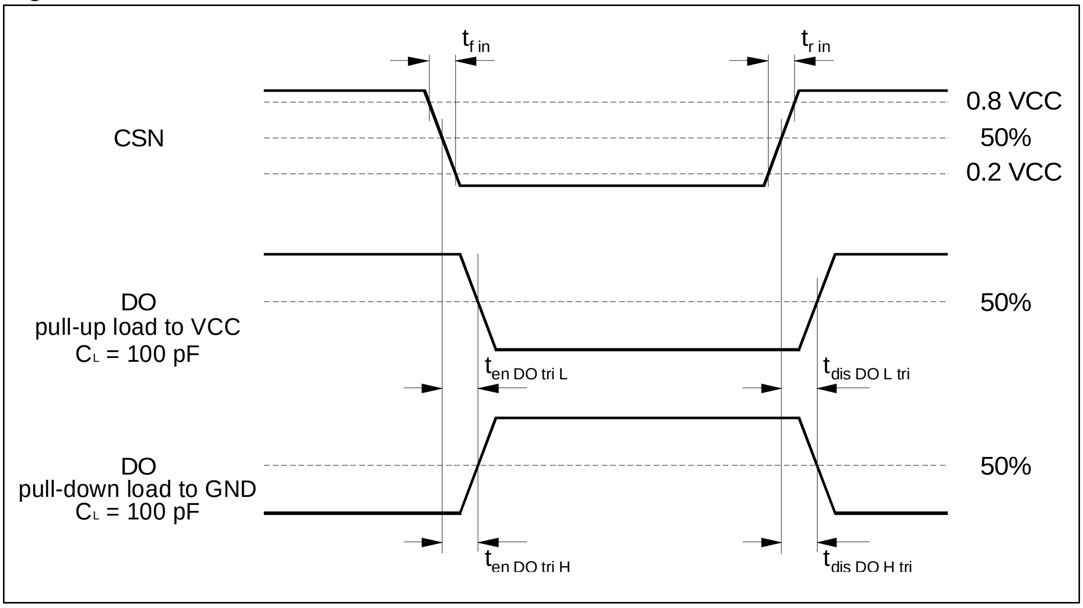


Figure 7. SPI - driver turn on / off timing, minimum CSN HI time

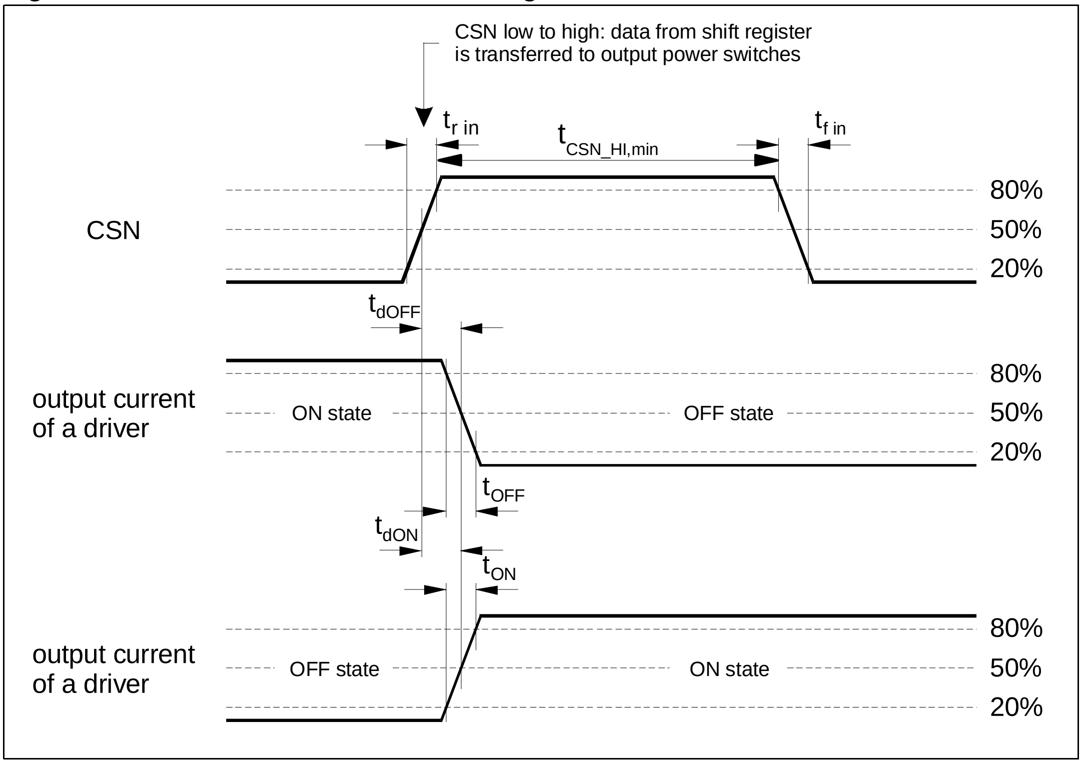
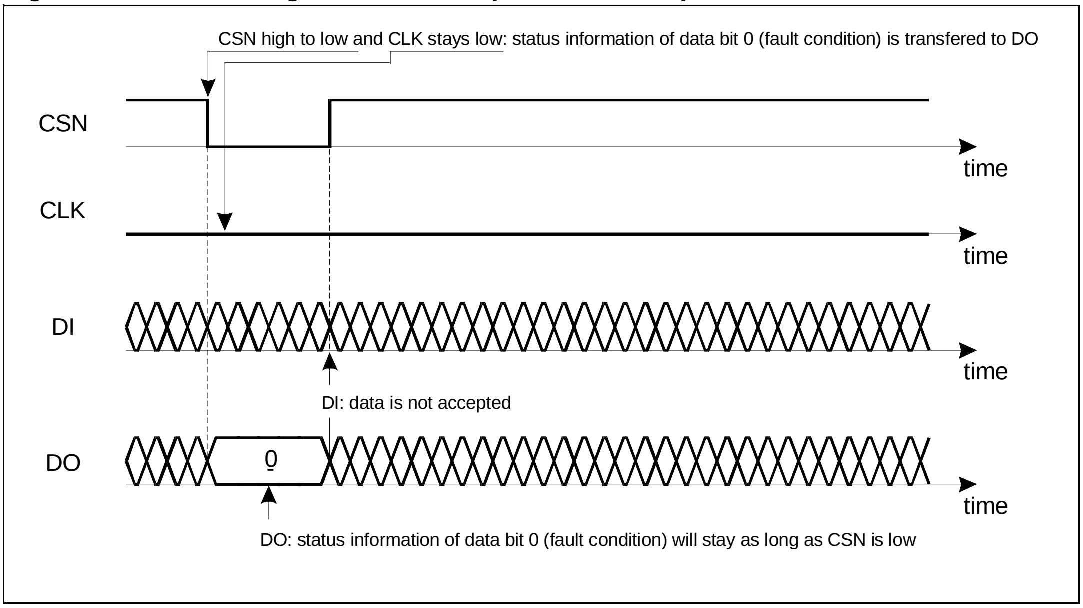


Figure 8. SPI - timing of status bit 0 (fault condition)



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges and the highside drivers. An internal charge-pump is used to drive the highside switches. The logic supply voltage V_{CC} (stabilized 5 V) is used for the logic part and the SPI of the device.

Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (V_{CC} increases from undervoltage to $V_{POR\ OFF}$ = 4.2 V) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 3.4 V), the outputs are switched to tristate (high impedance) and the status registers are cleared.

3.2 Standby mode

The standby mode of the L9954 is activated by clearing the bit 23 of the Input Data Register 0. All latched data will be cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at V_S (V_{CC}) is less than 6 µA (50µA) for CSN = high (DO in tristate). By switching the V_{CC} voltage a very low quiescent current can be achieved. If bit 23 is set, the device will be switched to active mode.

3.3 Inductive loads

Each half bridge is built by an internally connected highside and a lowside power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT3 without external free-wheeling diodes. The highside drivers OUT4 to OUT6 are intended to drive resistive loads. Hence only a limited energy (E<1mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L>100µH) an external free-wheeling diode connected to GND and the corresponding output is needed.

3.4 Diagnostic functions

All diagnostic functions (over/open load, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least 32 µs (open load: 1ms, respectively) before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. Open load and temperature warning function are intended for information purpose and will not change the state of the output drivers. On contrary, the overload condition will disable the corresponding driver (over-current) and overtemperature will switch off all drivers (thermal shutdown). Without setting the over-current recovery bits in the Input Data register, the microcontroller has to clear the over-current status bits to reactivate the corresponding drivers.

3.5 Overvoltage and undervoltage detection

If the power supply voltage V_S rises above the overvoltage threshold $V_{SOV\ OFF}$ (typical 21 V), the outputs OUT1 to OUT6 are switched to high impedance state to protect the load. When the voltage V_S drops below the undervoltage threshold $V_{SUV\ OFF}$ (UV-switch-OFF voltage), the output stages are switched to the high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S recovers (register 0: bit 20=0) to normal operating voltage the outputs stages return to the programmed state after at least 32 µs.

If the undervoltage/overvoltage recovery disable bit is set, the automatic turn-on of the drivers is deactivated. The microcontroller needs to clear the status bits to reactivate the drivers. It is strongly recommended to set bit 20 to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

3.6 Charge pump

The charge pump runs under all conditions in normal mode. In standby the charge pump is out of action.

3.7 Temperature warning and thermal shutdown

If junction temperature rises above $T_{j\ TW}$ a temperature warning flag is set after at least 32 µs and is detectable via the SPI. If junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit will be set and power DMOS transistors of all output stages are switched off to protect the device after at least 32 µs. Temperature warning flag and thermal shutdown bit are latched and must be cleared by the microcontroller. The related bit is only cleared if the temperature decreases below the trigger temperature. If the thermal shutdown bit has been cleared the output stages are reactivated.

3.8 Open-load detection

The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.

3.9 Over load detection

In case of an over-current condition a flag is set in the status register in the same way as open load detection. If the over-current signal is valid for at least t_{ISC} = 32 µs, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.10 Current monitor

The current monitor output sources a current image at the current monitor output which has a fixed ratio (1/10000) of the instantaneous current of the selected highside driver. Signal at output CM is blanked after switching on of driver until correct settlement of circuitry (at least for 32 µs).

The bits 18 and 19 of the Input Data Register 0 control which of the outputs OUT1, OUT4, OUT5 and OUT6 will be multiplexed to the current monitor output. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example this can be used to detect the motor state (starting, free-running, stalled). Moreover, it is possible to regulate the power of the defroster more precise by measuring the load current. The current monitor output is bidirectional (c.f. PWM inputs).

3.11 PWM inputs

Each driver has a corresponding PWM enable bit which can be programmed by the SPI interface. If the PWM enable bit in Input Data Register 1 is set , the output is controlled by the logically AND-combination of the PWM signal and the output control bit in Input Data Register 0. The outputs OUT1-OUT4 and OUT6 are controlled by the PWM1 input and the output OUT5 is controlled by the bidirectional input CM/PMW2. For example, the two PWM inputs can be used to dim two lamps independently by external PWM signals.

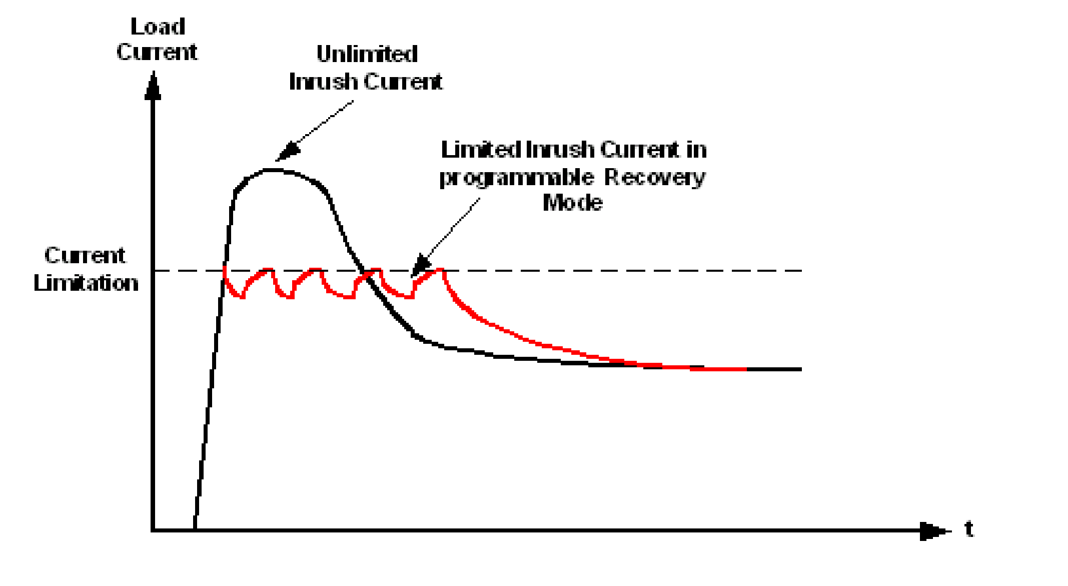
3.12 Cross-current protection

The three half-bridges of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge will be automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver will be changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver will start to conduct.

3.13 Programmable softstart function to drive loads with higher inrush current

Loads with start-up currents higher than the over-current limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable softstart function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device will automatically switch-on the outputs again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to be about 15% ...25%. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.5 kHz or 3 kHz. The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example the microcontroller can switch on light bulbs by setting the over-current recovery bit for the first 50ms. After clearing the recovery bit the output will be automatically disabled if the overload condition still exits.

Figure 9. Example of programmable softstart function for inductive loads



4 Functional description of the SPI

4.1 Serial Peripheral Interface (SPI)

This device uses a standard SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect the status bit 0 (fault condition) of the device which is a logical-or of all bits in the status registers 0 and 1. The microcontroller can poll the status of the device without the need of a full SPI-communication cycle.

*Note: In contrast to the SPI-standard the least significant bit (LSB) will be transferred first (see **Figure 3**).*

4.2 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal will activate the output driver and a serial communication can be started. The state when CSN is going low until the rising edge of CSN will be called a communication frame. If the CSN-input pin is driven above 7.5V, the L9954 will go into a test mode. In the test mode the DO will go from tri-state to active mode.

4.3 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.4 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

4.5 Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal.

4.6 Input data register

The device has two input registers. The first bit (bit 0) at the DI-input is used to select one of the two Input Registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Input Data Register only if a frame of exact 24 data bits are detected. Depending on bit 0 the contents of the selected status register will be transferred to DO during the current communication frame. Bit 1-17 controls the behavior of the corresponding driver.

If bit 23 is zero, the device will go into the standby-mode. The bits 18 and 19 are used to control the current monitor multiplexer. Bit 22 is used to reset all status bits in both status registers. The bits in the status registers will be cleared after the current communication frame (rising edge of CSN).

4.7 Status register

This devices uses two status registers to store and to monitor the state of the device. No error bit (bit 0) is used as a fault bit and is a logical-NOR combination of bits 1-22 in both status registers. The state of this bit can be polled by the microcontroller without the need of a full SPI-communication cycle. If one of the over-current bits is set, the corresponding driver will be disabled. If the over-current recovery bit of the output is not set the microcontroller has to clear the over-current bit to enable the driver. If the thermal shutdown bit is set, all drivers will go into a high impedance state. Again the microcontroller has to clear the bit to enable the drivers.

4.8 SPI - Input data and status registers

Table 18. SPI - input data and status registers 0

<table>
<tr><th rowspan="2">Bit</th><th colspan="5">Input register 0 (write)</th><th colspan="2">Status register 0 (read)</th></tr>
<tr><th colspan="2">Name</th><th colspan="3">Comment</th><th>Name</th><th>Comment</th></tr>
<tr><td>23</td><td colspan="2">Enable bit</td><td colspan="3">If Enable Bit is set the device switches in active mode. If Enable Bit is cleared the device goes into standby mode and all bits are cleared. After power-on reset device starts in standby mode.</td><td>Always 1</td><td>A broken VCC-or SPI-connection of the L9954 can be detected by the microcontroller, because all 24 bits low or high is not a valid frame.</td></tr>
<tr><td>22</td><td colspan="2">Reset bit</td><td colspan="3">If Reset Bit is set both status registers will be cleared after rising edge of CSN input.</td><td>V_S overvoltage</td><td rowspan="3">In case of an overvoltage or undervoltage event the corresponding bit is set and the outputs are deactivated. If VS voltage recovers to normal operating conditions outputs are reactivated automatically (if Bit 20 of status register 0 is not set).</td></tr>
<tr><td rowspan="2">21</td><td colspan="2">OC recovery duty cycle</td><td colspan="3" rowspan="2">This bit defines in combination with the over-current recovery bit (Input Register 1) the duty cycle in over-current condition of an activated driver.</td><td rowspan="2">V_S undervoltage</td></tr>
<tr><td>0: 12%</td><td>1: 25%</td></tr>
<tr><td>20</td><td colspan="2">Overvoltage/ Undervoltage recovery disable</td><td colspan="3">If this bit is set the microcontroller has to clear the status register after undervoltage / overvoltage event to enable the outputs.</td><td>Thermal shutdown</td><td>In case of a thermal shutdown all outputs are switched off.
The microcontroller has to clear the TSD bit by setting the Reset Bit to reactivate the outputs.</td></tr>
<tr><td>19</td><td colspan="2" rowspan="7">Current monitor select bits</td><td colspan="3">Depending on combination of bit 18 and 19 the current image (1/10.000) of the selected HS-output will be
multiplexed to the CM output:</td><td>Temperature warning</td><td>The TW bit can be used for thermal management
by the microcontroller to avoid a thermal shutdown. The microcontroller has to clear the TW bit.</td></tr>
<tr><td rowspan="6">18</td><td>Bit 19</td><td>Bit 18</td><td>Output</td><td rowspan="6">Not ready bit</td><td rowspan="6">After switching the device from standby mode to active mode an internal timer is started to allow chargepump to settle before the outputs can be activated. This bit is cleared automatically after start up time has finished. Since this bit is controlled by internal clock it can be used for synchronizing testing events (e.g. measuring filter times).</td></tr>
<tr><td>0</td><td>0</td><td>OUT6</td></tr>
<tr><td>1</td><td>0</td><td>OUT1</td></tr>
<tr><td>0</td><td>1</td><td>OUT4</td></tr>
<tr><td>1</td><td>1</td><td>OUT5</td></tr>
<tr><td colspan="3"></td></tr>
</table>

Table 18. SPI - input data and status registers 0 (continued)

Bit	Input register 0 (write)		Status register 0 (read)	
	Name	Comment	Name	Comment
17	OUT6 – HS on/off	If a bit is set the selected output driver is switched on. If the corresponding PWM enable bit is set (Input Register 1) the driver is only activated if PWM1 (PWM2) input signal is high. The outputs of OUT1-OUT3 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from VS to GND.	OUT6 – HS over-current	In case of an over-current event the corresponding status bit is set and the output driver is disabled. If the over-current Recovery Enable bit is set (Input Register 1) the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (Bit 21). If the over-current recovery bit is not set the microcontroller has to clear the over-current bit (Reset Bit) to reactivate the output driver.
16	x (don't care)		0	
15	OUT5 – HS on/off		OUT5 – HS over-current	
14	OUT4 – HS on/off		OUT4 – HS over-current	
13	x (don't care)		0	
12	x (don't care)		0	
11	x (don't care)		0	
10	x (don't care)		0	
9	x (don't care)		0	
8	x (don't care)		0	
7	x (don't care)		0	
6	OUT3 – HS on/off		OUT3 – HS over-current	
5	OUT3 – LS on/off		OUT3 – LS over-current	
4	OUT2 – HS on/off		OUT2 – HS over-current	
3	OUT2 – LS on/off		OUT2 – LS over-current	
2	OUT1 – HS on/off		OUT1 – HS over-current	
1	OUT1 – LS on/off		OUT1 – LS over-current	
0	0		No error bit	A logical NOR-combination of all bits 1 to 22 in both status registers.

Table 19. SPI - input data and status registers 1

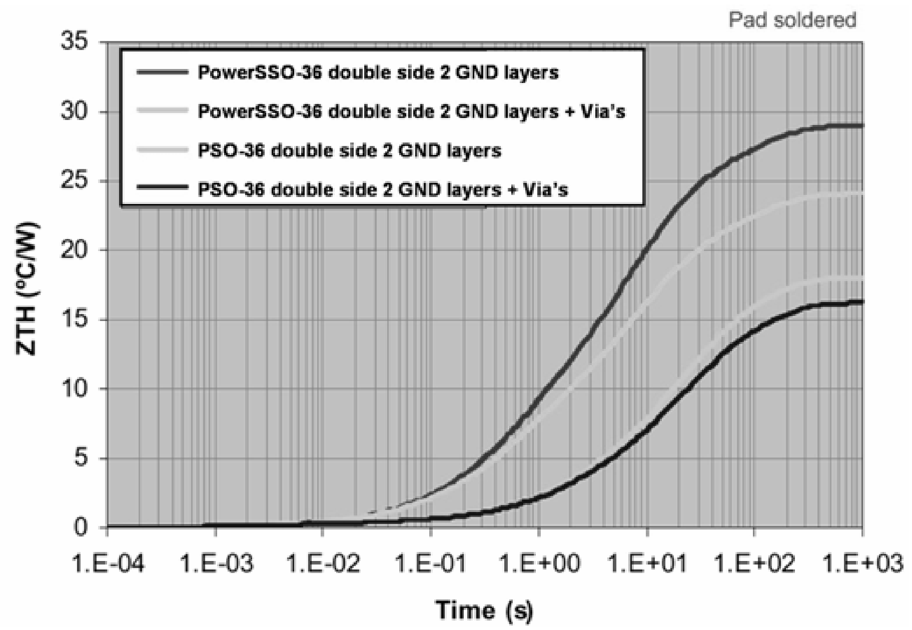
Bit	Input register 1 (write)		Status register 1 (read)	
	Name	Comment	Name	Comment
23	Enable bit	If Enable bit is set the device will be switched in active mode. If Enable Bit is cleared device goes into standby mode and all bits are cleared. After power-on reset device starts in standby mode.	Always 1	A broken VCC-or SPI-connection of the L9954 can be detected by the microcontroller, because all 24 bits low or high is not a valid frame.
22	OUT6 OC Recovery Enable	In case of an over-current event the over-current status bit (Status Register 0) is set and the output is switched off. If the over-current Recovery Enable bit is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (Bit 21 of Input Data Register 0). Depending on occurrence of Overcurrent Event and internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero.	VS overvoltage	In case of an overvoltage or undervoltage event the corresponding bit is set and the outputs are deactivated. If Vs voltage recovers to normal operating conditions outputs are reactivated automatically.
21	x (don’t care)		VS undervoltage	
20	OUT5 OC Recovery Enable		Thermal shutdown	In case of a thermal shutdown all outputs are switched off. The microcontroller has to clear the TSD bit by setting the Reset Bit to reactivate the outputs.
19	OUT4 OC Recovery Enable		Temperature warning	The TW bit can be used for thermal management by the microcontroller to avoid a thermal shutdown. The microcontroller has to clear the TW bit.
18	x (don’t care)		Not ready bit	After switching the device from standby mode to active mode an internal timer is started to allow chargepump to settle before the outputs can be activated. This bit is only present during start up time. Since this bit is controlled by internal clock it can be used for synchronizing testing events(e.g. measuring filter times).

Table 19. SPI - input data and status registers 1 (continued)

Bit	Input register 1 (write)		Status register 1 (read)	
	Name	Comment	Name	Comment
17	x (don't care)	After 50ms the bit can be cleared. If over-current condition still exists, a wrong load can be assumed.	OUT6 – HS open load	The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.
16	x (don't care)		0	
15	x (don't care)		OUT5 – HS open load	
14	OUT3 OC Recovery Enable		OUT4 – HS open load	
13	OUT2 OC Recovery Enable		0	
12	OUT1 OC Recovery Enable		0	
11	OUT6 PWM1 Enable	If the PWM1/2 Enable Bit is set and the output is enabled (Input Register 0) the output is switched on if PWM1/2 input is high and switched off if PWM1/2 input is low. OUT5 is controlled by PWM2 input. All other outputs are controlled by PWM1 input.	0	
10	x (don't care)		0	
9	OUT5 PWM2 Enable		0	
8	OUT4 PWM1 Enable		0	
7	x (don't care)		0	
6	x (don't care)		OUT3 – HS open load	
5	x (don't care)		OUT3 – LS open load	
4	x (don't care)		OUT2 –HS open load	
3	OUT3 PWM1 Enable		OUT2– LS open load	
2	OUT2 PWM1 Enable		OUT1 – HS open load	
1	OUT1 PWM1 Enable		OUT1 – LS open load	
0	1		No Error bit	A logical NOR-combination of all bits 1 to 22 in both status registers.

5 Packages thermal data

Figure 10. Packages thermal data



6 Package and packing information

6.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSO-36™ package information

Figure 11. PowerSO-36™ package dimensions

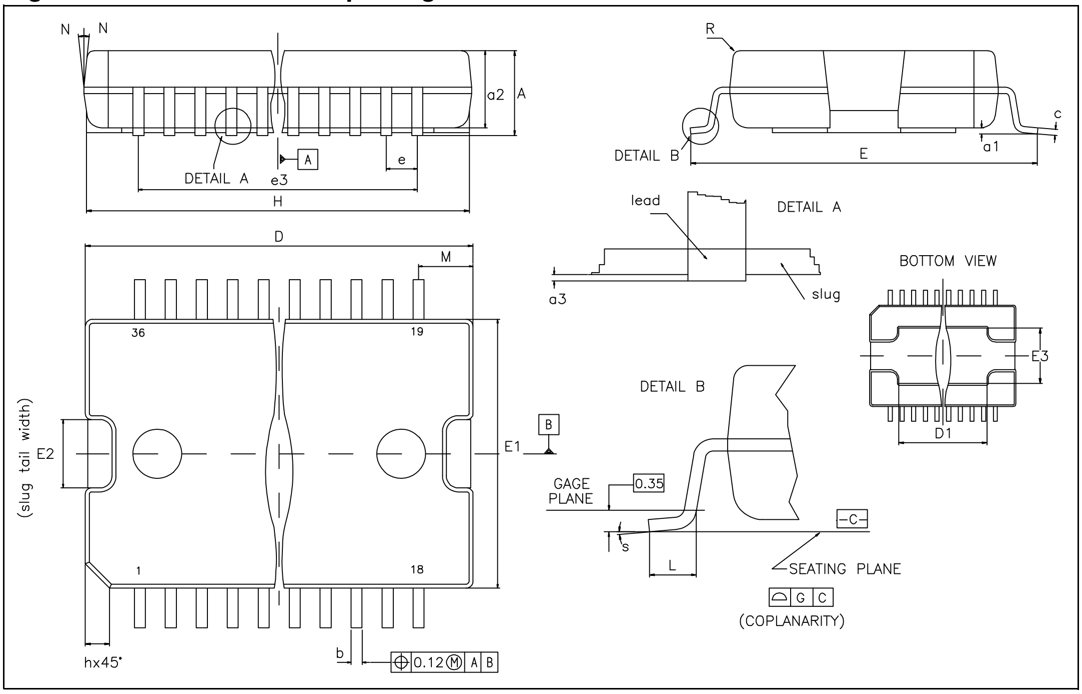


Table 20. PowerSO-36™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			3.60
a1	0.10		0.30
a2			3.30
a3	0		0.10
b	0.22		0.38
c	0.23		0.32
D *	15.80		16.00
D1	9.40		9.80
E	13.90		14.5
E1 *	10.90		11.10
E2			2.90
E3	5.80		6.20
e		0.65	
e3		11.05	
G	0		0.10
H	15.50		15.90
h			1.10
L	0.8		1.10
M			
N			10 deg
R			
s			8 deg

6.3 PowerSSO-36™ package information

Figure 12. PowerSSO-36™ package dimensions

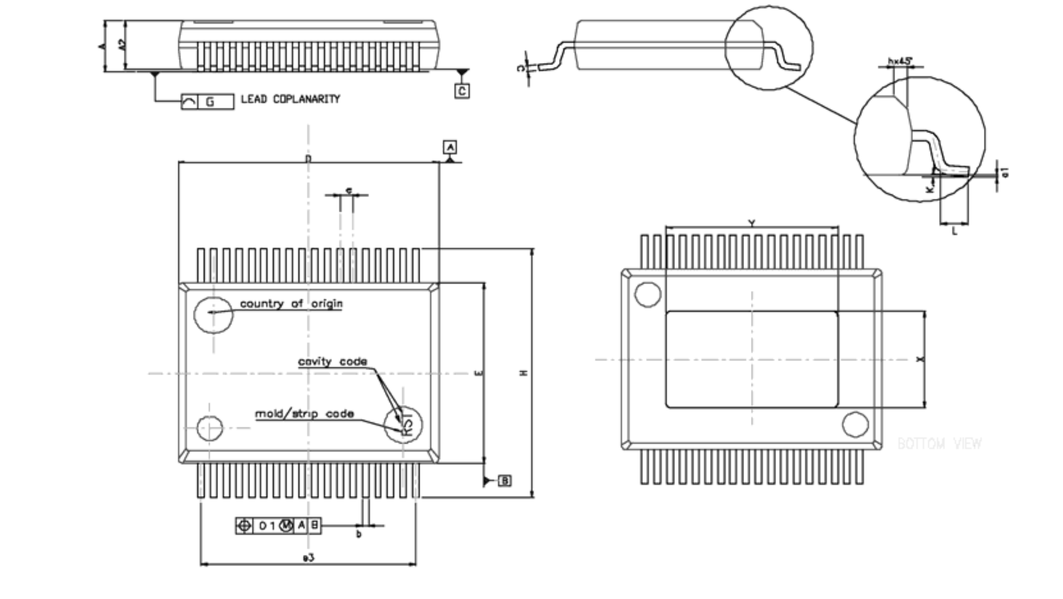


Table 21. PowerSSO-36™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	-	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D *	10.10	-	10.50
E *	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
N	-	-	10 deg

Table 21. PowerSSO-36™ mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
X	4.3	-	5.2
Y	6.9	-	7.5

6.4 PowerSO-36™ packing information

Figure 13. PowerSO-36™ tube shipment (no suffix)

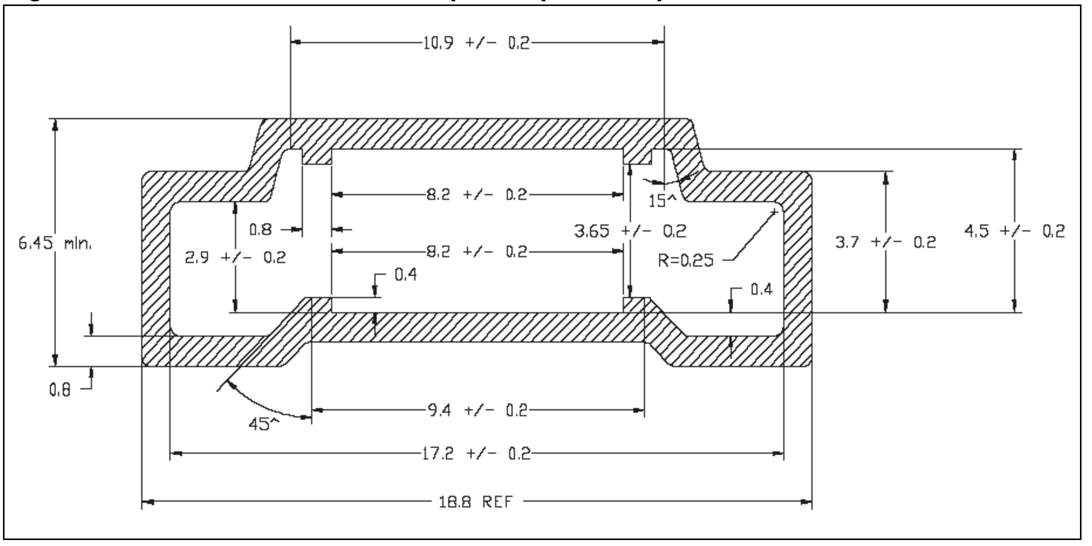
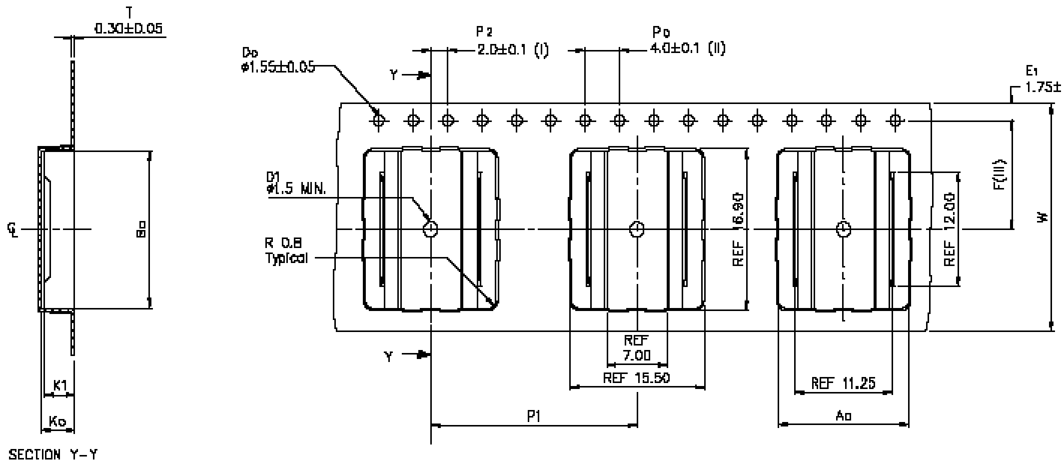
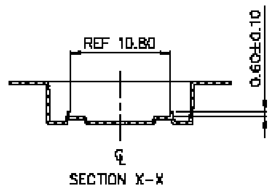


Figure 14. PowerSO-36™ tape and reel shipment (suffix "TR")





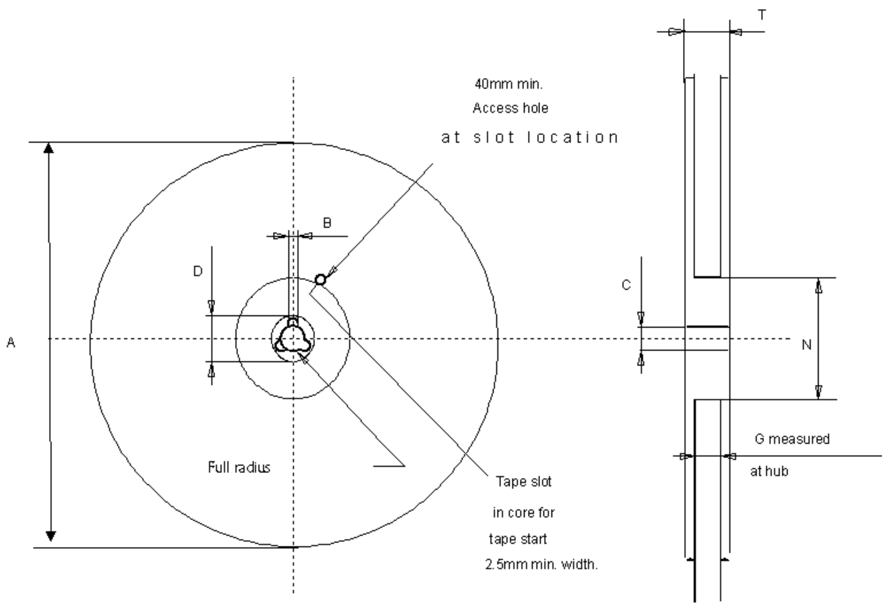
TAPE DIMENSIONS

A0	15.20 ± 0.1
B0	16.60 ± 0.1
K0	3.90 ± 0.1
K1	3.50 ± 0.1
F	11.50 ± 0.1
P1	24.00 ± 0.1
W	24.00 ± 0.3

All dimensions are in mm.

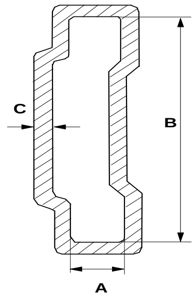
REEL DIMENSIONS

Base Qty	600
Bulk Qty	600
A (max)	330
B (min)	1.5
C (±0.2)	13
D (min)	20.2
G (+2 / -0)	24.4
N (min)	60
T (max)	30.4



6.5 PowerSSO-36™ packing information

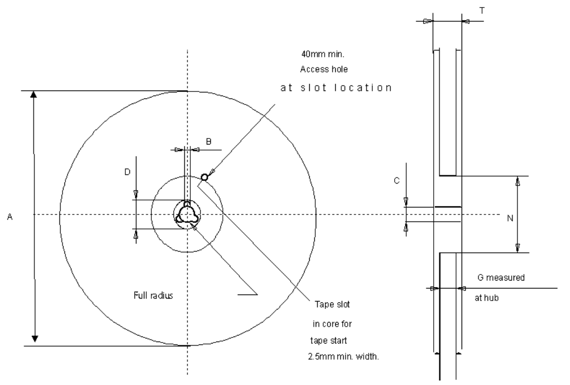
Figure 15. PowerSSO-36™ tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 16. PowerSSO-36™ tape and reel shipment (suffix "TR")

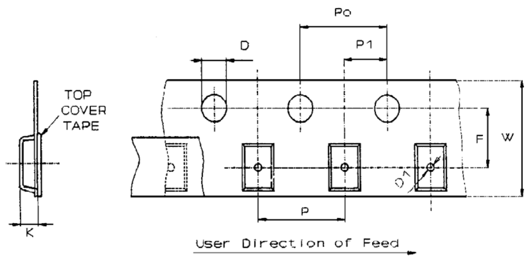


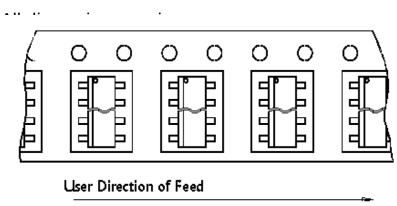
Reel dimensions

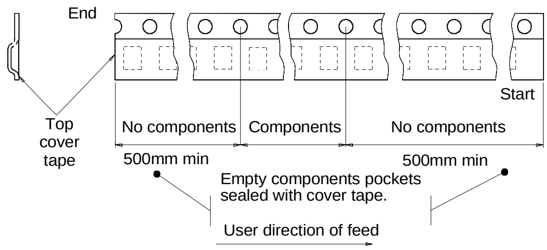
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Tape dimensions
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2







7 Revision history

Table 22. Document revision history

Date	Revision	Description of changes
23-Jan-2008	1	Initial release.
24-Jun-2009	2	*Table 21: PowerSSO-36™ mechanical data*: – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F and k rows
17-May-2010	3	*Table 21: PowerSSO-36™ mechanical data*: – Changed X: minimum value from 4.1 to 4.3 and maximum value from 4.7 to 5.2 – Changed Y: minimum value from 6.5 to 6.9 and maximum value from 7.1 to 7.5
22-Sep-2013	4	Updated Disclaimer.