TUSB564 USB TYPE-C™ DP Alt Mode 8.1 Gbps Sink-Side Linear Redriver Crosspoint Switch

1 Features

- USB Type-C™ crosspoint switch supporting
  - USB 3.1 Gen 1 + 2 DP 1.4 lanes
  - 4 DP 1.4 lanes
- USB 3.1 Gen 1 up to 5 Gbps
- DisplayPort 1.4 up to 8.1 Gbps (HBR3)
- VESA DisplayPort™ alt mode UFP_D redriving crosspoint switch supporting c, d, and e pin assignments
- Ultra-low-power architecture
- Linear redriver with up to 12 dB equalization
- Transparent to DisplayPort link training
- Automatic LFPS de-emphasis control to meet USB 3.1 certification requirements
- Configuration through GPIO or I^2C
- Hot-plug capable
- Industrial temperature range: –40ºC to 85ºC (TUSB564I)
- Commercial temperature range: 0ºC to 70ºC (TUSB564)
- 4 mm x 6 mm, 0.4 mm Pitch WQFN package

2 Applications

- Monitors
- HDTV
- Projectors
- Docking stations

3 Description

The TUSB564 s a VESA USB Type-C™ Alt Mode redriving switch supporting USB 3.1 data rates up to 5 Gbps and DisplayPort 1.4 up to 8.1 Gbps for upstream facing port (Sink). The device is used for UFP_D pin assignments C, D, and E from the VESA DisplayPort Alt Mode on USB Type-C Standard.

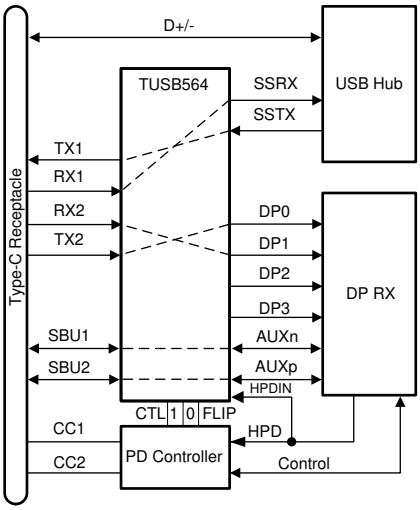
The TUSB564 provides several levels of receive linear equalization to compensate for inter symbol interference (ISI) due to cable and board trace loss. Operates on a single 3.3-V supply and comes in a commercial temperature range and industrial temperature range.

Device Information(1)

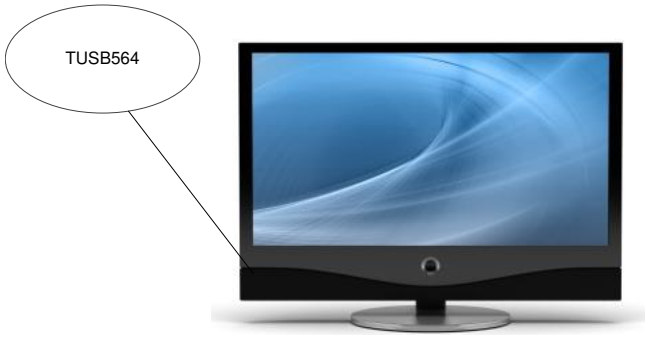
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB564	WQFN (40)	4.00 mm x 6.00 mm
TUSB564I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematics



TUSB564 Use-Case Example



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2019) to Revision F — **Page**

- Added note to disable AUX snoop to resolve interop issues with a non-compliant AUX source. ... 18

Changes from Revision D (November 2018) to Revision E — **Page**

- Added following to pin 38 description: If I2C_EN = “F”, then this pin must be set to “F” or “0”. ... 5
- Changed G_{LF} min, typ, and max values from -1, 0, 1 to -2.5, 0.5, and 3.5 respectively ... 9
- Added $G_{LF\_LFPS\_TX1/2}$ parameter to AC electrical ... 9

Changes from Revision C (February 2018) to Revision D — **Page**

- Changed the RNQ pin image appearance ... 4
- Changed the EN pin Description in the *Pin Functions* table ... 5
- Changed the HPDIN pin From: I/O To: 2 Level I ... 5
- Added pull-down indicator (PD) in the I/O column on FLIP/SCL and CTL0/SDA pins ... 5
- Added Junction temperature to absolute maximum ratings table ... 6
- From: Internal pull-down resistance for CTL1. To: Internal pull-down resistance for CTL1, CTL0, FLIP, and EN ... 7
- Deleted EN from Note 1 of Table 8 ... 24

Changes from Revision B (January 2018) to Revision C — **Page**

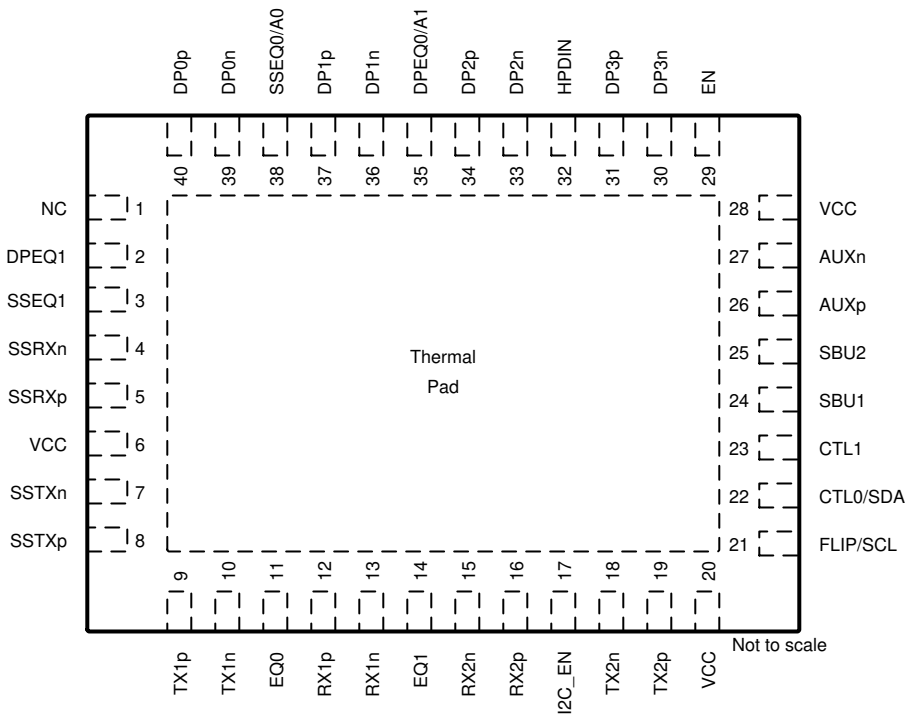
- Changed the column on EN From: I To: 2 Level I (PD) ... 5
- Updated AUX_SBU_OVR Description field in Table 15 to match Table 6 ... 28

Changes from Original (October 2017) to Revision A **Page**

- Changed the device status from *Advance Information* to *Production Data* 1
- From: UFP_D pin assignments C, and D To: UFP_D pin assignments C, D, and E 1
- Added Note which describes AUX snoop feature is only supported in I2C mode. In GPIO mode, AUX snoop is disabled and all four lanes are enabled. 18

5 Pin Configuration and Functions

RNQ Package
40-Pin (WQFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DP0p	40	Diff O	DP Differential positive output for DisplayPort Lane 0.
DP0n	39	Diff O	DP Differential negative output for DisplayPort Lane 0.
DP1p	37	Diff O	DP Differential positive output for DisplayPort Lane 1.
DP1n	36	Diff O	DP Differential negative output for DisplayPort Lane 1.
DP2p	34	Diff O	DP Differential positive output for DisplayPort Lane 2.
DP2n	33	Diff O	DP Differential negative output for DisplayPort Lane 2.
DP3p	31	Diff O	DP Differential positive output for DisplayPort Lane 3.
DP3n	30	Diff O	DP Differential negative output for DisplayPort Lane 3.
TX1n	10	Diff I/O	Differential negative input for DisplayPort or differential negative output for USB3.1 upstream facing port.
TX1p	9	Diff I/O	Differential positive input for DisplayPort or differential positive output for USB3.1 upstream facing port.
RX1n	13	Diff I	Differential negative input for DisplayPort or USB3.1 upstream facing port.
RX1p	12	Diff I	Differential positive input for DisplayPort or USB 3.1 upstream facing port.
RX2p	16	Diff I	Differential positive input for DisplayPort or USB 3.1 upstream facing port.
RX2n	15	Diff I	Differential negative input for DisplayPort or USB 3.1 upstream facing port.
TX2p	19	Diff I/O	Differential positive input for DisplayPort or differential positive output for USB3.1 upstream Facing port.
TX2n	18	Diff I/O	Differential negative input for DisplayPort or differential negative output for USB3.1 upstream Facing port.
SSTXp	8	Diff I	Differential positive input for USB3.1 downstream facing port.
SSTXn	7	Diff I	Differential negative input for USB3.1 downstream facing port.
SSRXp	5	Diff O	Differential positive output for USB3.1 downstream facing port.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SSRXn	4	Diff O	Differential negative output for USB3.1 downstream facing port.
EQ1	14	4 Level I	This pin along with EQ0 sets the USB receiver equalizer gain for upstream facing RX1 and RX2 when USB used. Up to 11dB of EQ available.
EQ0	11	4 Level I	This pin along with EQ1 sets the USB receiver equalizer gain for upstream facing RX1 and RX2 when USB used. Up to 11 dB of EQ available.
EN	29	2 Level I (PD)	Device Enable, when I2C_EN = '0'. Device disable function not used when I2C_EN ≠ '0'. L = Device Disabled H = Device Enabled On rising edge of EN pin, the device will sample all 4-level inputs including the I2C_EN pin. EN pin will not reset the I^2C registers.
HPDIN	32	2 Level I	Hot Plug Detect. This pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled while the AUX to SBU switch will remain closed.
I2C_EN	17	4 Level I	I^2C Programming Mode or GPIO Programming Select. I2C is only disabled when this pin is '0'. 0 = GPIO mode (I^2C disabled) R = TI Test Mode (I^2C enabled at 3.3 V) F = I^2C enabled at 1.8 V 1 = I^2C enabled at 3.3 V.
SBU1	24	I/O, CMOS	SBU1. This pin should be DC coupled to the SBU1 pin on the Type-C receptacle. A 2-M ohm resistor to GND is also recommended.
SBU2	25	I/O, CMOS	SBU2. This pin should be DC coupled to the SBU2 pin on the Type-C receptacle. A 2-M ohm resistor to GND is also recommended.
AUXp	26	I/O, CMOS	AUXp. DisplayPort AUX positive I/O connected to the DisplayPort sink through a AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 1M resistor to DP_PWR (3.3 V). This pin along with AUXN is used by the TUSB564 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
AUXn	27	I/O, CMOS	AUXn. DisplayPort AUX negative I/O connected to the DisplayPort sink through a AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 1M resistor to GND. This pin along with AUXP is used by the TUSB564 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
DPEQ1	2	4 Level I	DisplayPort Receiver EQ. This along with DPEQ0 will select the DisplayPort receiver equalization gain.
DPEQ0/A1	35	4 Level I	DisplayPort Receiver EQ. This along with DPEQ1 will select the DisplayPort receiver equalization gain. When I2C_EN ≠ '0', this pin will also set the TUSB564 I^2C address.
SSEQ1	3	4 Level I	Along with SSEQ0, sets the USB receiver equalizer gain for downstream facing SSTXP/N.
SSEQ0/A0	38	4 Level I	Along with SSEQ1, sets the USB receiver equalizer gain for downstream facing SSTXP/N. When I2C_EN ≠ '0', this pin will also set the TUSB564 I^2C address. If I2C_EN = "F", then this pin must be set to "F" or "0".
FLIP/SCL	21	2 Level I (Failsafe) (PD)	When I2C_EN = '0' this is Flip control pin, otherwise this pin is I^2C clock. . When used for I^2C clock pullup to I^2C master's VCC I2C supply.
CTL0/SDA	22	2 Level I (Failsafe) (PD)	When I2C_EN = '0' this is a USB3.1 Switch control pin, otherwise this pin is I^2C data. When used for I^2C data pullup to I^2C master's VCC I2C supply.
CTL1	23	2 Level I (Failsafe) (PD)	DP Alt mode Switch Control Pin. When I2C_EN = '0', this pin will enable or disable DisplayPort functionality. Otherwise, when I2C_EN ≠ '0', DisplayPort functionality is enabled and disabled through I^2C registers. L = DisplayPort Disabled. H = DisplayPort Enabled.
VCC	6, 20, 28	P	3.3-V Power Supply
NC	1	NC	No connect pin. Leave open.
GND	Thermal Pad	G	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature and voltage range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage Range	-0.3	4	V
V_{IN_DIFF}	Differential Voltage at Differential Inputs		±2.5	V
V_{IN_SE}	Input Voltage at Differential Inputs	-0.5	4	V
V_{IN_CMOS}	Input Voltage at CMOS Inputs	-0.3	4	V
T_J	TUSB564 Junction Temperature		110	°C
	TUSB564I Junction Temperature		125	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature and voltage range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature for TUSB564	0		70	°C
T_A	Ambient temperature for TUSB564I	-40		85	°C
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CC_RAMP}	Power supply ramp	0.1		100	ms
V_{I2C}	Supply that external resistors on SDA and SCL are pulled up to	1.7		3.6	V
V_{PSN}	Power supply noise on VCC			100	mV

6.4 Thermal Information

THERMAL METRIC(1)		TUSB564 RNQ (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 ELECTRICAL CHARACTERISTICS

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
$P_{CC-ACTIVE-USB}$	Average active power in USB-only mode while in U0.	CTL1 = L; CTL0 = H; Link in U0 at 5Gbps;		330		mW
$P_{CC-ACTIVE-USB-DP}$	Average active power in USB + 2 lane DP mode.	CTL1 = H; CTL0 = H; USB in U0 at 5Gbps; DP at 8.1Gbps;		660		mW
$P_{CC-ACTIVE-DP}$	Average active power in 4 lane DP mode.	CTL1 = H; CTL0 = L; Four DP lanes at 8.1Gbps		660		mW
$P_{CC-NC-USB}$	Average power in USB mode while in disconnect state.	CTL1 = L; CTL0 = H; No USB device detected;		2.5		mW
$P_{CC-U2U3}$	Average power in USB mode while in U2/U3 state	CTL1 = L; CTL0 = H; Link in U2 or U3;		2.5		mW
$P_{CC-SHUTDOWN}$	Average power in Shutdown mode.	CTL1 = L; CTL0 = L; I2C_EN = "0";		0.7		mW
4-State CMOS Inputs(EQ[1:0], SSEQ[1:0], DPEQ[1:0], I2C_EN)						
I_{IH}	High-level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	20		80	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	-160		-40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3 V		0.55		V
	Threshold R/ Float	V_{CC} = 3.3 V		1.65		V
	Threshold Float / 1	V_{CC} = 3.3 V		2.7		V
R_{PU}	Internal pull up resistance			45		kΩ
R_{PD}	Internal pull-down resistance			95		kΩ
2-State CMOS Input (CTL0, CTL1, FLIP, EN, HPDIN) CTL1, CTL0 and FLIP are Failsafe						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
R_{PD}	Internal pull-down resistance for CTL1, CTL0, FLIP, and EN.			500		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V	-25		25	µA
I_{IL}	Low-level input current	V_{IN} = GND, V_{CC} = 3.6 V	-25		25	µA
I2C Control Pins SCL, SDA						
V_{IH}	High-level input voltage	I2C_EN ! = 0	0.7 x V_{I2C}		3.6	V
V_{IL}	Low-level input voltage	I2C_EN ! = 0	0		0.3 × V_{I2C}	V
V_{OL}	Low-level output voltage	I2C_EN ! = 0; I_{OL} = 3 mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN ! = 0; V_{OL} = 0.4 V	20			mA
I_{i_I2C}	Input current on SDA pin	0.1 × V_{I2C} < Input voltage < 3.3 V	-10		10	µA
C_{i_I2C}	Input capacitance				10	pF
USB Differential Receiver (RX1P/N, RX2P/N, SSTXP/N)						
$V_{RX-DIFF-PP}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		2000		mVpp
$V_{RX-DC-CM}$	Common-mode voltage bias in the receiver (DC)			0		V
$R_{RX-DIFF-DC}$	Differential input impedance (DC)	Present after a USB3.1 device is detected on TXP/TXN	72		120	Ω
$R_{RX-CM-DC}$	Receiver DC Common Mode impedance	Present after a USB3.1 device is detected on TXP/TXN	18		30	Ω

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{RX-HIGH-IMP-DC-POS}$	Common-mode input impedance with termination disabled (DC)	Present when no USB3.1 device is detected on TXP/TXN. Measured over the range of 0-500 mV with respect to GND.	25			kΩ
$V_{SIGNAL-DET-DIFF-PP}$	Input Differential peak-to-peak Signal Detect Assert Level	at 5Gbps, No loss and bit rate PRBS7 pattern		70		mV
$V_{RX-IDLE-DET-DIFF-PP}$	Input Differential peak-to-peak Signal Detect De-assert Level	at 5 Gbps, No loss and bit rate PRBS7 pattern		50		mV
$V_{RX-LFPS-DET-DIFF-PP}$	Low-frequency Periodic Signaling (LFPS) Detect Threshold	Below the minimum is squelched.	100		300	mV
C_{RX}	RX input capacitance to GND	At 2.5 GHz		0.5	1	pF
$RL_{RX-DIFF}$	Differential Return Loss	50 MHz – 1.25 GHz at 90 Ω		-16		dB
		2.5 GHz at 90 Ω		-17		dB
RL_{RX-CM}	Common Mode Return Loss	50 MHz – 2.5 GHz at 90 Ω		-12		dB
EQ_{SSP}	Receiver equalization	SSEQ[1:0] and EQ[1:0] at 2.5 GHz.		12		dB
USB Differential Transmitter (TX1P/N, TX2P/N, SSRXP/N)						
$V_{TX-DIFF-PP}$	Transmitter dynamic differential voltage swing range.			1300		mVpp
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during Receiver Detection	at 3.3 V			600	mV
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS	measured at the connector side of the AC coupling caps with 50 Ω load	-600		600	mV
$V_{TX-DC-CM}$	Common-mode voltage bias in the transmitter (DC)		0		2	V
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC Common-mode voltage active	At 3.3V; Max mismatch from Txp+Txn for both time and amplitude			100	mVpp
$V_{TX-IDLE-DIFF-AC-PP}$	AC Electrical idle differential peak-to-peak output voltage	At package pins	0		10	mV
$V_{TX-IDLE-DIFF-DC}$	DC Electrical idle differential output voltage	At package pins after low-pass filter to remove AC component	0		14	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common mode voltage between U1 and U0	At package pin			200	mV
C_{TX}	TX input capacitance to GND	At 2.5 GHz			1.25	pF
$R_{TX-DIFF}$	Differential impedance of the driver		75		120	Ω
$C_{AC-COUPLING}$	AC Coupling capacitor		75		265	nF
R_{TX-CM}	Common-mode impedance of the driver	Measured with respect to AC ground over 0-500 mV	18		30	Ω
$I_{TX-SHORT}$	TX short circuit current	TX+/- shorted to GND			67	mA
$RL_{TX-DIFF}$	Differential Return Loss	50 MHz – 1.25 GHz at 90 Ω		-17		dB
$RL_{TX-DIFF-2.5G}$	Differential Return Loss	2.5 GHz at 90 Ω		-12		dB
RL_{TX-CM}	Common Mode Return Loss	50 MHz – 2.5 GHz at 90 Ω		-10		dB
AC Electrical Characteristics for USB and DP						
Crosstalk	Differential Cross Talk between TX and RX signal Pairs	at 2.5 GHz		-27		dB

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{LF}	Low-frequency voltage gain.	at 100 MHz, 600 mVpp V_{ID}	-2.5	0.5	3.5	dB
$G_{LF\_LFPS\_TX1/2}$	Low-frequency voltage gain for SSTX->TX1/TX2 path.	at 10 to 50MHz sine wave; 1.0Vpp V_{ID}; EQ = 0; FLIP = 0 and 1;	0	0.8	1.6	dB
$CP_{1\ dB-LF}$	Low-frequency 1-dB compression point	at 100 MHz, 200 mVpp < V_{ID} < 2000 mVpp		1000		mVpp
$CP_{1\ dB-HF}$	High-frequency 1-dB compression point	at 2.5 GHz, 200 mVpp < V_{ID} < 2000 mVpp		1000		mVpp
f_{LF}	Low-frequency cutoff	200 mVpp < V_{ID} < 2000 mVpp		20	50	kHz
D_{J_5G}	TX output deterministic jitter	200 mVpp < V_{ID} < 2000 mVpp, PRBS7, 5 Gbps		0.04		UIpp
$D_{J\_8.1G}$	TX output deterministic jitter	200 mVpp < V_{ID} < 2000 mVpp, PRBS7, 8.1 Gbps		0.08		UIpp
T_{J_5G}	TX output total jitter	200 mVpp < V_{ID} < 2000 mVpp, PRBS7, 5 Gbps		0.07		UIpp
$T_{J\_8.1G}$	TX output total jitter	200 mVpp < V_{ID} < 2000 mVpp, PRBS7, 8.1 Gbps		0.12		UIpp
DisplayPort Receiver (TX1P/N, TX2P/N, RX1P/N, RX2P/N)						
V_{ID_PP}	Peak-to-peak input differential dynamic voltage range			2000		mV
V_{IC}	Input Common Mode Voltage			0		V
C_{AC}	AC coupling capacitance		75		265	nF
EQ_{DP}	Receiver Equalizer	DPEQ1, DPEQ0 at 4.05 GHz		12		dB
d_R	Data rate	HBR3			8.1	Gbps
R_{ti}	Input Termination resistance		80	100	120	Ω
DisplayPort Transmitter (DP[3:0]P/N)						
$V_{TX-DIFFPP}$	VOD dynamic range			1300		mV
$I_{TX-SHORT}$	TX short circuit current	TX+/- shorted to GND			67	mA
AUXP/N and SBU1/2						
R_{ON}	Output ON resistance	V_{CC} = 3.3 V; V_{IN} = 0 to 0.4 V for AUXP; V_{IN} = 2.7 V to 3.6 V for AUXN		5	10	Ω
$R_{ON-MISMATCH}$	ΔON resistance mismatch within pair	V_{CC} = 3.3 V; V_{IN} = 0 to 0.4 V for AUXP; V_{IN}= 2.7 V to 3.6 V for AUXN			1	Ω
R_{ON_FLAT}	ON resistance flatness (RONmax–RON min) measured at identical VCC and temperature	V_{CC} = 3.3 V; V_{IN} = 0 to 0.4 V for AUXP; V_{IN} = 2.7 V to 3.6 V for AUXN			2	Ω
$V_{AUXP\_DC\_CM}$	AUX Channel DC common mode voltage for AUXP and SBU2.	V_{CC} = 3.3 V	0		0.4	V
$V_{AUXN\_DC\_CM}$	AUX Channel DC common mode voltage for AUXN and SBU1	V_{CC} = 3.3 V	2.7		3.6	V
C_{AUX_ON}	ON-state capacitance	V_{CC} = 3.3 V; CTL1 = 1; V_{IN} = 0 V or 3.3 V		4	7	pF
C_{AUX_OFF}	OFF-state capacitance	V_{CC} = 3.3 V; CTL1 = 0; V_{IN} = 0 V or 3.3 V		3	6	pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUXp/n and SBU1/2						
T_{AUX_PD}	Switch propagation delay				1400	ps
$T_{AUX\_SW\_OFF}$	Switching time CTL1 to switch OFF. Not including $T_{CTL1\_DEBOUNCE}$.				7500	ns
$T_{AUX\_SW\_ON}$	Switching time CTL1 to switch ON				3000	ns
T_{AUX_INTRA}	Intra-pair output skew				400	ps
USB3.1 and DisplayPort mode transition requirement (GPIO mode)						
$T_{GP\_USB\_4DP}$	Min overlap of CTL0 and CTL1 when transitioning from USB 3.1 only mode to 4-Lane DisplayPort mode or vice versa		4			µs
$T_{CTL1\_DEBOUNCE}$	CTL1 and HPDIN debounce time when transitioning from H to L		3		10	ms
I2C (SDA and SCL)						
f_{SCL}	I2C clock frequency				1	MHz
t_{BUF}	Bus free time between START and STOP conditions		0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.26			µs
t_{LOW}	Low period of the I2C clock		0.5			µs
t_{HIGH}	High period of the I2C clock		0.26			µs
t_{SUSTA}	Setup time for a repeated START condition		0.26			µs
t_{HDDAT}	Data hold time		0			µs
t_{SUDAT}	Data setup time		50			ns
t_R	Rise time of both SDA and SCL signals				120	ns
t_F	Fall time of both SDA and SCL signals		$20 \times (V_{I2C}/5.5\ V)$		120	ns
t_{SUSTO}	Setup time for STOP condition		0.26			µs
C_b	Capacitive load for each bus line				100	pF

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
USB 3.1					
$t_{IDLEEntry}$,	Delay from U0 to electrical idle		10		ns
$t_{IDLEExit\_U1}$	U1 exist time: break in electrical idle to the transmission of LFPS		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS		10		µs
t_{RXDET_INTVL}	RX detect interval while in Disconnect			12	ms
$t_{IDLEExit\_DISC}$	Disconnect Exit Time		10		µs
t_{Exit_SHTDN}	Shutdown Exit Time (CTL0 = V_{CC}/2 to U2/U3)		1		ms
t_{DIFF_DLY}	Differential Propagation Delay (20%-80% of differential voltage measured 1.7 inch from the output pin)			300	ps
$t_{PWRUPACTIVE}$	Time when Vcc reaches 70% to device active			1	ms
t_R, t_F	Output Rise/Fall Time		40		ps
t_{RF-MM}	Output Rise/Fall time mismatch (20%-80% of differential voltage measured 1.7 inch from the output pin)			5	ps

6.8 Typical Characteristics

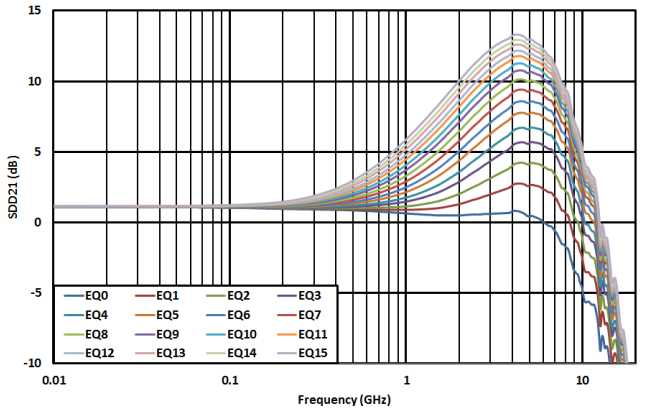


Figure 1. DisplayPort EQ Settings Curves

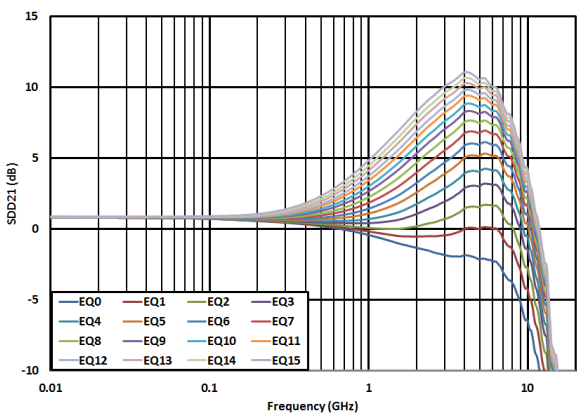


Figure 2. USB RX (DFP) EQ Settings Curves

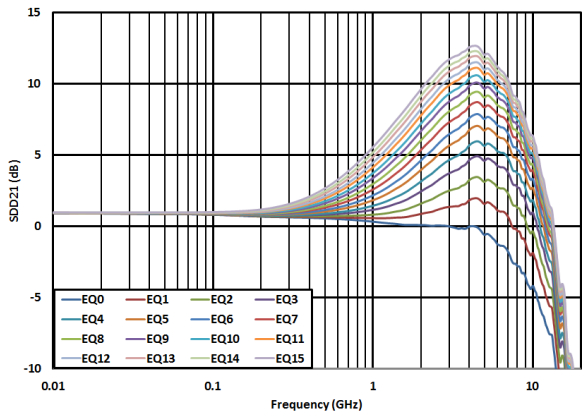


Figure 3. USB TX (UFP) EQ Settings Curves

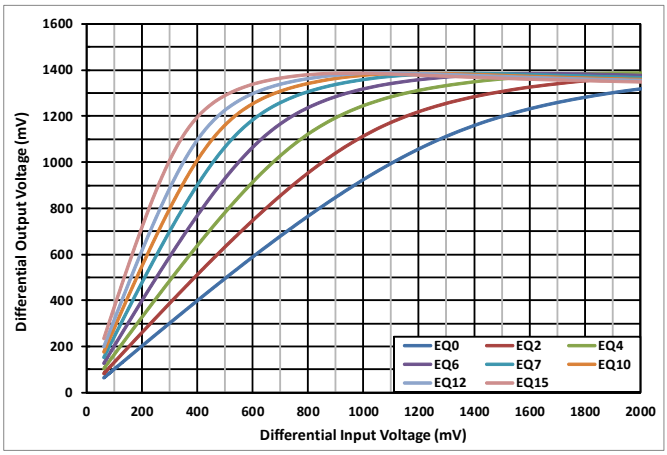


Figure 4. DisplayPort Linearity Curves at 4.05 GHz

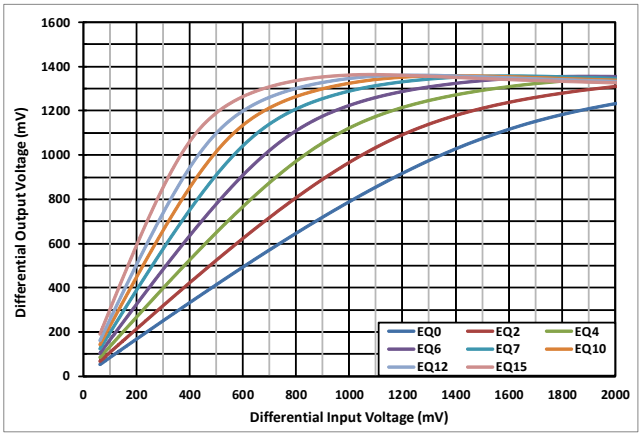


Figure 5. USB TX (DFP) Linearity Curves at 2.5 GHz

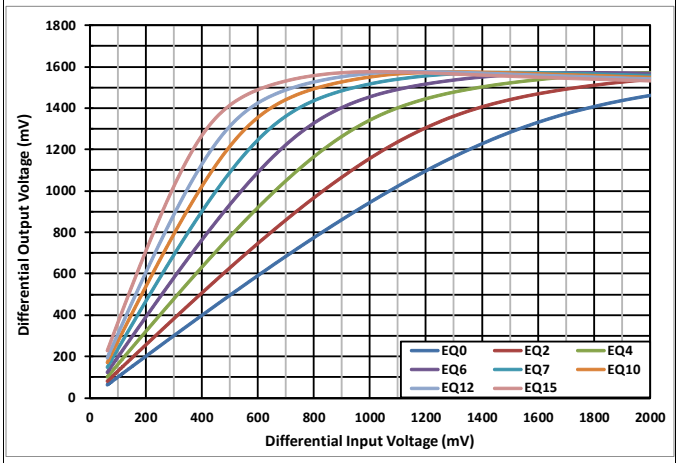


Figure 6. USB RX (UFP) Linearity Curves at 2.5 GHz

Typical Characteristics (continued)

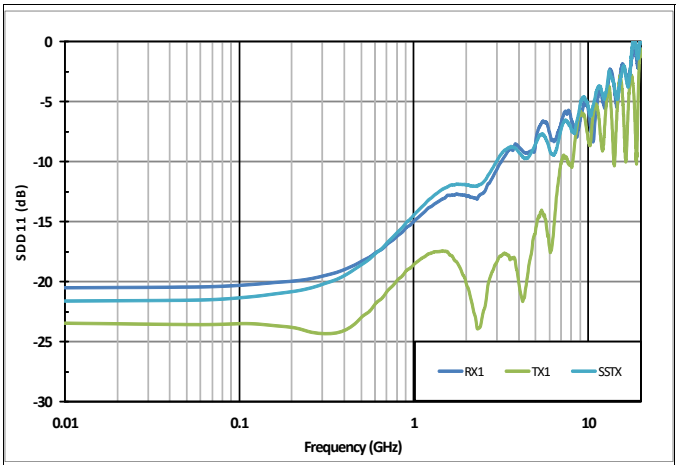


Figure 7. Input Return Loss Performance

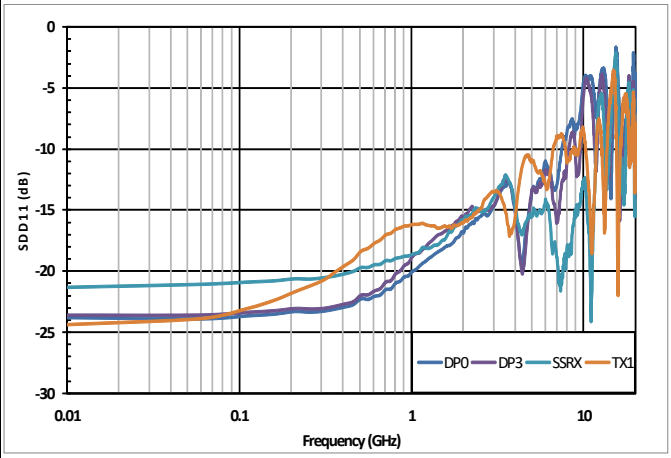


Figure 8. Output Return Loss Performance

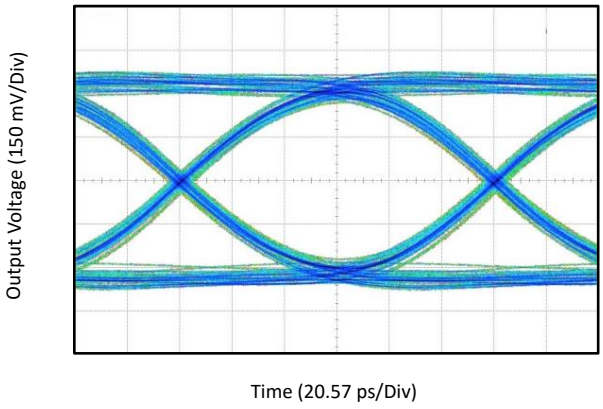


Figure 9. DisplayPort HBR3 Eye-Pattern Performance with 12-inch Input PCB Trace at 8.1 Gbps

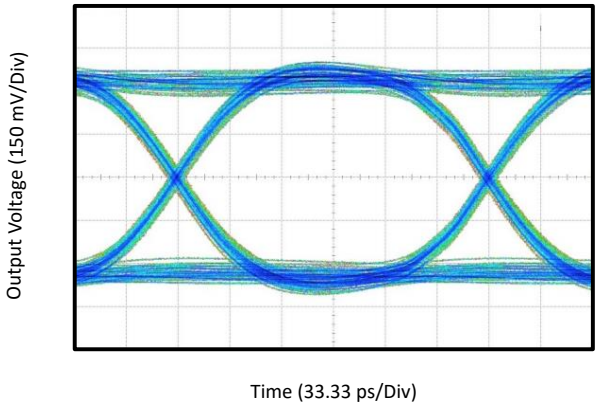


Figure 10. USB 3.1 Gen1 Eye-Pattern Performance with 12-inch Input PCB Trace at 5 Gbps

7 Parameter Measurement Information

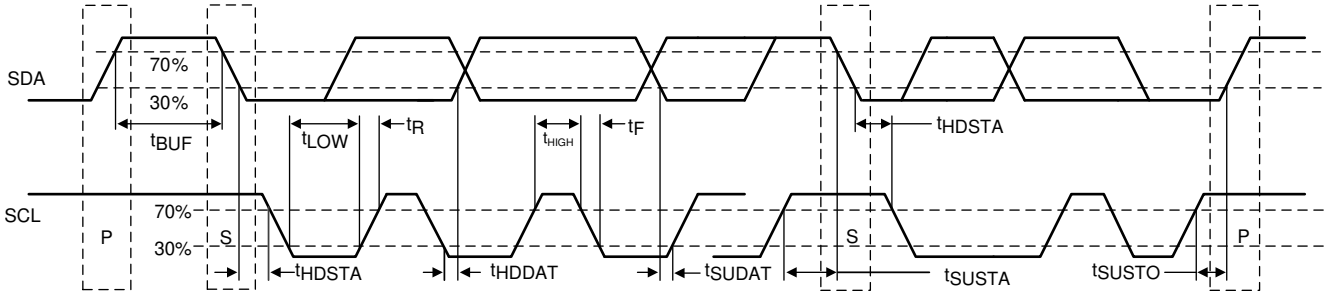


Figure 11. I²C Timing Diagram Definitions

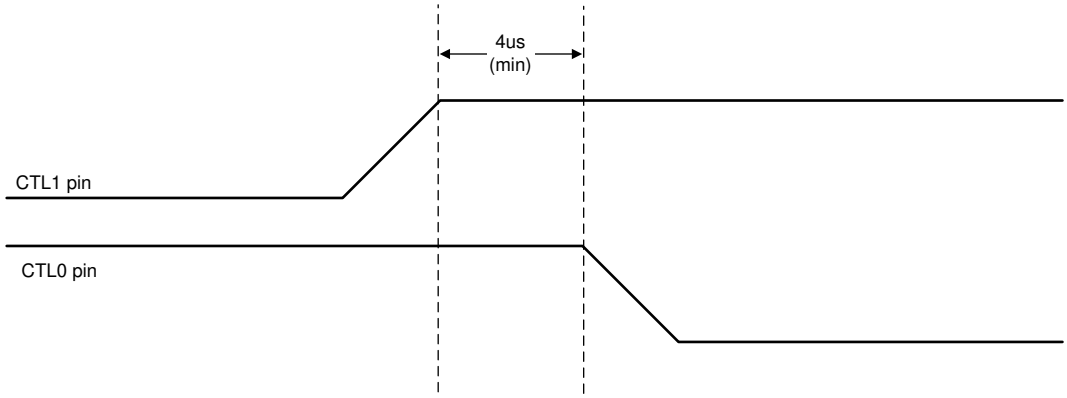


Figure 12. USB3.1 to 4-Lane DisplayPort in GPIO Mode

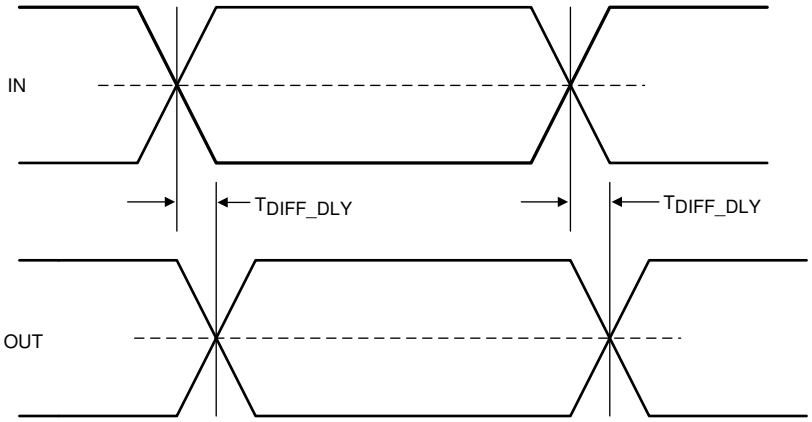


Figure 13. Propagation Delay

Parameter Measurement Information (continued)

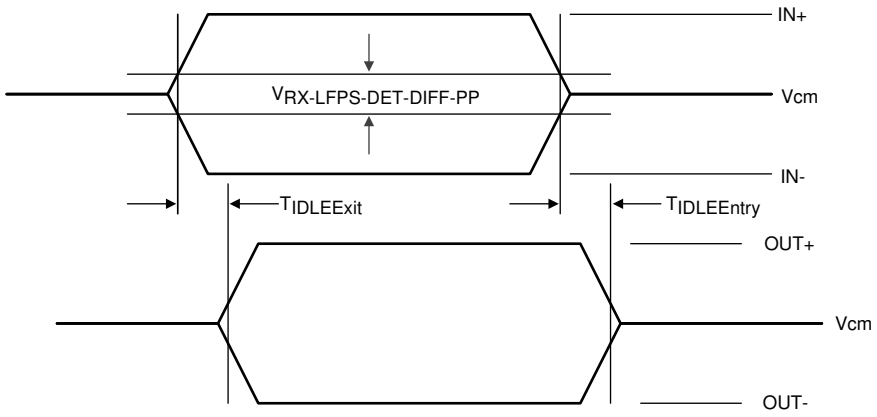


Figure 14. Electrical Idle Mode Exit and Entry Delay

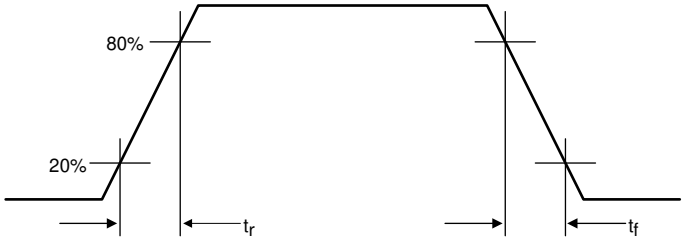


Figure 15. Output Rise and Fall Times

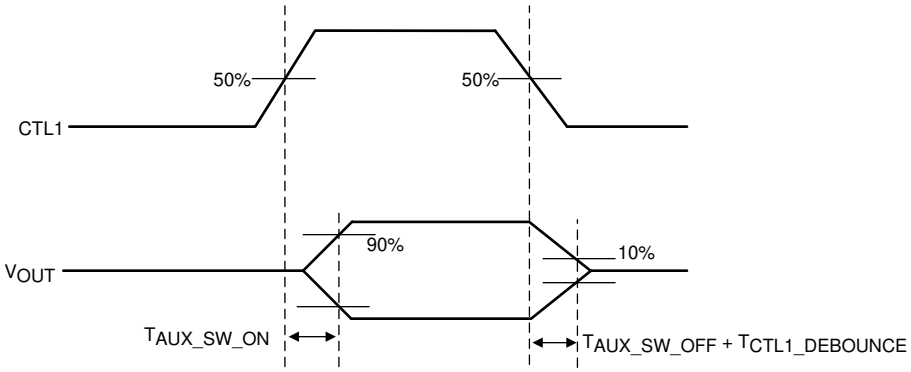


Figure 16. AUX and SBU Switch ON and OFF Timing Diagram

8 Detailed Description

8.1 Overview

The TUSB564 is a VESA USB Type-C Alt Mode redriving switch supporting data rates up to 8.1 Gbps for upstream facing port. This device uses 5th generation USB redriver technology. The device is used for UFP pin assignments C and D from the VESA DisplayPort Alt Mode on USB Type-C Standard.

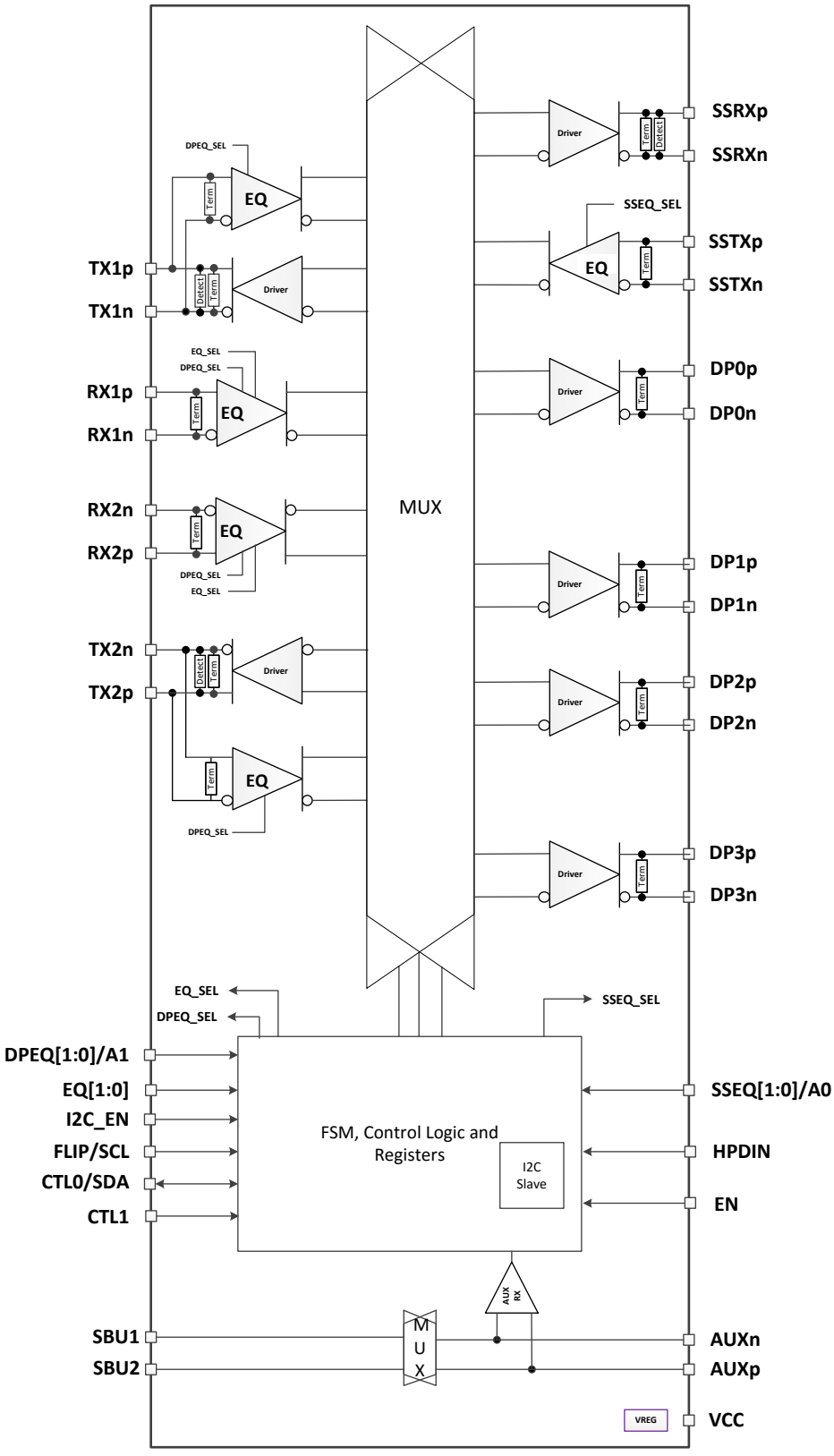
The TUSB564 provides several levels of receive equalization to compensate for cable and board trace loss which if not equalized causes inter-symbol interference (ISI) when USB 3.1 Gen 1 or DisplayPort 1.4 signals travel across a PCB or cable. This device requires a 3.3-V power supply. It comes in a commercial temperature range and industrial temperature range.

For a sink application, the TUSB564 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.1 Gen 1 and DisplayPort version 1.4 HBR3. The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. The equalization should be set based on the amount of insertion loss in the channels connected to the TUSB564. Independent equalization control for each channel can be set using EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pins.

The TUSB564 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB564 periodically performs receiver detection on the TX pairs. If it detects a USB 3.1 receiver, the RX termination is enabled, and the TTUSB564 is ready to re-drive.

The device ultra-low-power architecture operates at a 3.3-V power supply and achieves Enhanced performance. The automatic LFPS De-Emphasis control further enables the system to be USB3.1 compliant.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB 3.1

The TUSB564 supports USB 3.1 Gen 1 datarates up to 5 Gbps. The TUSB564 supports all the USB defined power states (U0, U1, U2, and U3). Because the TUSB564 is a linear redriver, it can't decode USB3.1 physical layer traffic. The TUSB564 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.1 interface.

The TUSB564 features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB564 enables receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1_SEL, EQ2_SEL, and SSEQ_SEL registers.

8.3.2 DisplayPort

The TUSB564 supports up to 4 DisplayPort lanes at datarates up to 8.1Gbps (HBR3). The TUSB564, when configured in DisplayPort mode, monitors the native AUX traffic as it traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB564 manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB564 snoops native AUX writes to DisplayPort sink's DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE). TUSB564disables/enables lanes based on value written to LANE_COUNT_SET. The TUSB564 disables all lanes when SET_POWER_STATE is in the D3. Otherwise, active lanes are based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. Once AUX snoop is disabled, management of TUSB564 DisplayPort lanes are controlled through various configuration registers.

NOTE

AUX snooping feature is only supported when TUSB564 is configured for I2C mode. When TUSB564 is configured for GPIO mode, the AUX snoop feature is disabled and all four DP lanes are enabled if HPDIN is asserted high.

When TUSB564's AUX snoop feature is enabled, the syncs defined by the DisplayPort standard must be received in order for AUX snoop feature to function properly. AUX writes to panel's DPCD address 0x00600 and 0x00101 should result in SET_POWER_STATE and LANE_COUNT_SET fields at TUSB564's offset 0x12 to get set to the appropriate value. If these fields do not get set correctly, then incoming AUX may not be compliant. If this is the case, then it is best to disable AUX snoop by setting the AUX_SNOOP_DISABLE field at offset 0x13.

8.3.3 4-level Inputs

The TUSB564 has (I2C_EN, EQ[1:0], DPEQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TUSB564 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal 35 kΩ pull-up and a 95 kΩ pull-down. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5%to V_{CC}. Option 2: Tie directly to V_{CC}.

NOTE

All four-level inputs are latched on rising edge of internal reset. After t_{cfg_hd}, the internal pull-up and pull-down resistors will be isolated in order to save power.

8.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and the resulting inter-symbol interference in the system before the input or after the output of the TUSB564. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss. Two 4-level input pins enable up to 16 possible equalization settings. USB3.1 upstream path, USB3.1 downstream path, and DisplayPort each have their own two 4-level inputs. The TUSB564 also provides the flexibility of adjusting settings through I^2C registers.

8.4 Device Functional Modes

8.4.1 Device Configuration in GPIO Mode

The TUSB564 is in GPIO configuration when I2C_EN = “0”. The TUSB564 supports the following configurations: USB 3.1 only, 2 DisplayPort lanes + USB 3.1, or 4 DisplayPort lanes (no USB 3.1). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB 3.1 only, 2 lanes of DisplayPort, or 4-lanes of DisplayPort as detailed in Table 2. The AUXp or AUXn to SBU1 or SBU2 mapping is controlled based on Table 3.

After power-up (V_{CC} from 0 V to 3.3 V), the TUSB564 defaults to USB3.1 mode. The USB PD controller upon detecting no device attached to Type-C port or USB3.1 operation not required by attached device must take TUSB564 out of USB3.1 mode by transitioning the CTL0 pin from L to H and back to L.

Table 2. GPIO Configuration Control

CTL1 PIN	CTL0 PIN	FLIP PIN	CONFIGURATION	VESA DisplayPort ALT MODE UFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
L	H	H	One Port USB 3.1 – With Flip	—
H	L	L	4 Lane DP - No Flip	C
H	L	H	4 Lane DP – With Flip	C
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D

Table 3. GPIO AUXp or AUXn to SBU1 or SBU2 Mapping

CTL1 PIN	FLIP PIN	MAPPING
H	L	SBU1 → AUXn SBU2 → AUXp
H	H	SBU2 → AUXn SBU1 → AUXp
L > 2 ms	X	Open

Table 4 details the TUSB564 mux routing. This table is valid for both I^2C and GPIO configuration modes.

Table 4. INPUT to OUTPUT Mapping

CTL1 PIN	CTL0 PIN	FLIP PIN	FROM	TO
			INPUT PIN	OUTPUT PIN
L	L	L	NA	NA
L	L	H	NA	NA
L	H	L	RX1p	SSRXp
			RX1n	SSRXn
			SSTXp	TX1p
			SSTXn	TX1n
L	H	H	RX2p	SSRXp
			RX2n	SSRXn
			SSTXp	TX2p
			SSTXn	TX2n
H	L	L	TX2p	DP0p
			TX2n	DP0n
			RX2p	DP1p
			RX2n	DP1n
			RX1p	DP2p
			RX1n	DP2n
			TX1p	DP3p
			TX1n	DP3n
H	L	H	TX1p	DP0p
			TX1n	DP0n
			RX1p	DP1p
			RX1n	DP1n
			RX2p	DP2p
			RX2n	DP2n
			TX2p	DP3p
			TX2n	DP3n
H	H	L	RX1p	SSRXp
			RX1n	SSRXn
			SSTXp	TX1p
			SSTXn	TX1n
			TX2p	DP0p
			TX2n	DP0n
			RX2p	DP1p
			RX2n	DP1n
H	H	H	RX2p	SSRXp
			RX2n	SSRXn
			SSTXp	TX2p
			SSTXn	TX2n
			TX1p	DP0p
			TX1n	DP0n
			RX1p	DP1p
			RX1n	DP1n

8.4.2 Device Configuration In I²C Mode

The TUSB564 is in I²C mode when I2C_EN is not equal to "0". The same configurations defined in GPIO mode are also available in I²C mode. The TUSB564 USB3.1 and DisplayPort configuration is controlled based on Table 5. The AUXp or AUXn to SBU1 or SBU2 mapping control is based on Table 6.

Table 5. I²C Configuration Control

REGISTERS			CONFIGURATION	VESA DisplayPort ALT MODE UFP_D CONFIGURATION
CTLSEL1	CTLSEL0	FLIPSEL		
0	0	0	Power Down	—
0	0	1	Power Down	—
0	1	0	One Port USB 3.1 - No Flip	—
0	1	1	One Port USB 3.1 – With Flip	—
1	0	0	4 Lane DP - No Flip	C
1	0	1	4 Lane DP – With Flip	C
1	1	0	One Port USB 3.1 + 2 Lane DP- No Flip	D
1	1	1	One Port USB 3.1 + 2 Lane DP– With Flip	D

Table 6. I²C AUXp or AUXn to SBU1 or SBU2 Mapping

REGISTERS			MAPPING
AUX_SBU_OVR	CTLSEL1	FLIPSEL	
00	1	0	SBU1 → AUXn SBU2 → AUXp
00	1	1	SBU2 → AUXn SBU1 → AUXp
00	0	X	Open
01	X	X	SBU1 → AUXn SBU2 → AUXp
10	X	X	SBU2 → AUXn SBU1 → AUXp
11	X	X	Open

8.4.3 DisplayPort Mode

The TUSB564 supports up to four DisplayPort lanes at datarates up to 8.1 Gbps. TUSB564 can be enabled for DisplayPort through GPIO control pin CTL1 or through I²C register CTLSEL1. When I2C_EN is '0', DisplayPort is controlled based on Table 2. When not in GPIO mode, DisplayPort functionality is controlled through I²C registers. Data transfer through the DisplayPort lanes is further controlled by the HPDIN pin. DisplayPort needs to be enabled using CTL1 pin or CTLSEL1 register and also HPDIN needs to be pulled high for the DisplayPort data trasfer to be enabled through the DisplayPort lanes.

8.4.4 Linear EQ Configuration

Each of the TUSB564 receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I^2C registers or through GPIOs. Table 7 details the gain value for each available combination when TUSB564 is in GPIO mode. These same options are also available in I^2C mode by updating registers DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, DP3EQ_SEL, EQ1_SEL, EQ2_SEL, and SSEQ_SEL. Each of the 4-bit EQ configuration registers is mapped to the configuration pins as follows: x_SEL = {x1[1:0],x0[1:0]} where xn[1:0] are the EQ configuration pins with pin levels mapped to 2-bit values as: 0 = 00, R = 01, F = 10, 1 = 11.

Table 7. TUSB564 Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 UPSTREAM FACING PORTS			USB 3.1 DOWNSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	-0.9	0	0	-2.4	0	0	-0.3
1	0	R	0.2	0	R	-1.3	0	R	1.6
2	0	F	1.2	0	F	-0.4	0	F	3.0
3	0	1	2.2	0	1	0.7	0	1	4.4
4	R	0	3.1	R	0	1.5	R	0	5.4
5	R	R	4.0	R	R	2.5	R	R	6.5
6	R	F	4.8	R	F	3.2	R	F	7.3
7	R	1	5.6	R	1	4.0	R	1	8.1
8	F	0	6.3	F	0	4.8	F	0	8.9
9	F	R	7.0	F	R	5.5	F	R	9.5
10	F	F	7.5	F	F	6.0	F	F	10.0
11	F	1	8.1	F	1	6.6	F	1	10.6
12	1	0	8.5	1	0	7.1	1	0	11.0
13	1	R	9.1	1	R	7.6	1	R	11.4
14	1	F	9.5	1	F	8.0	1	F	11.8
15	1	1	9.9	1	1	8.5	1	1	12.1

8.4.5 USB3.1 Modes

The TUSB564 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.1 interface, the TUSB564 can be in one of four primary modes of operation when USB 3.1 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB564 has not detected far-end termination on upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB564 remains in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB564 immediately exits this mode and enter U0 once far-end termination is detected.

Once in U0 mode, the TUSB564 will redrive all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB564 remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB564 immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB564 UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB564 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB564 leaves the U2/U3 mode and transitions to the Disconnect mode. It also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB564 immediately transitions to the U0 mode. In U2/U3 mode, the TUSB564 receiver terminations remain enabled but the TX DC common mode voltage is not maintained.

8.4.6 Operation Timing – Power Up

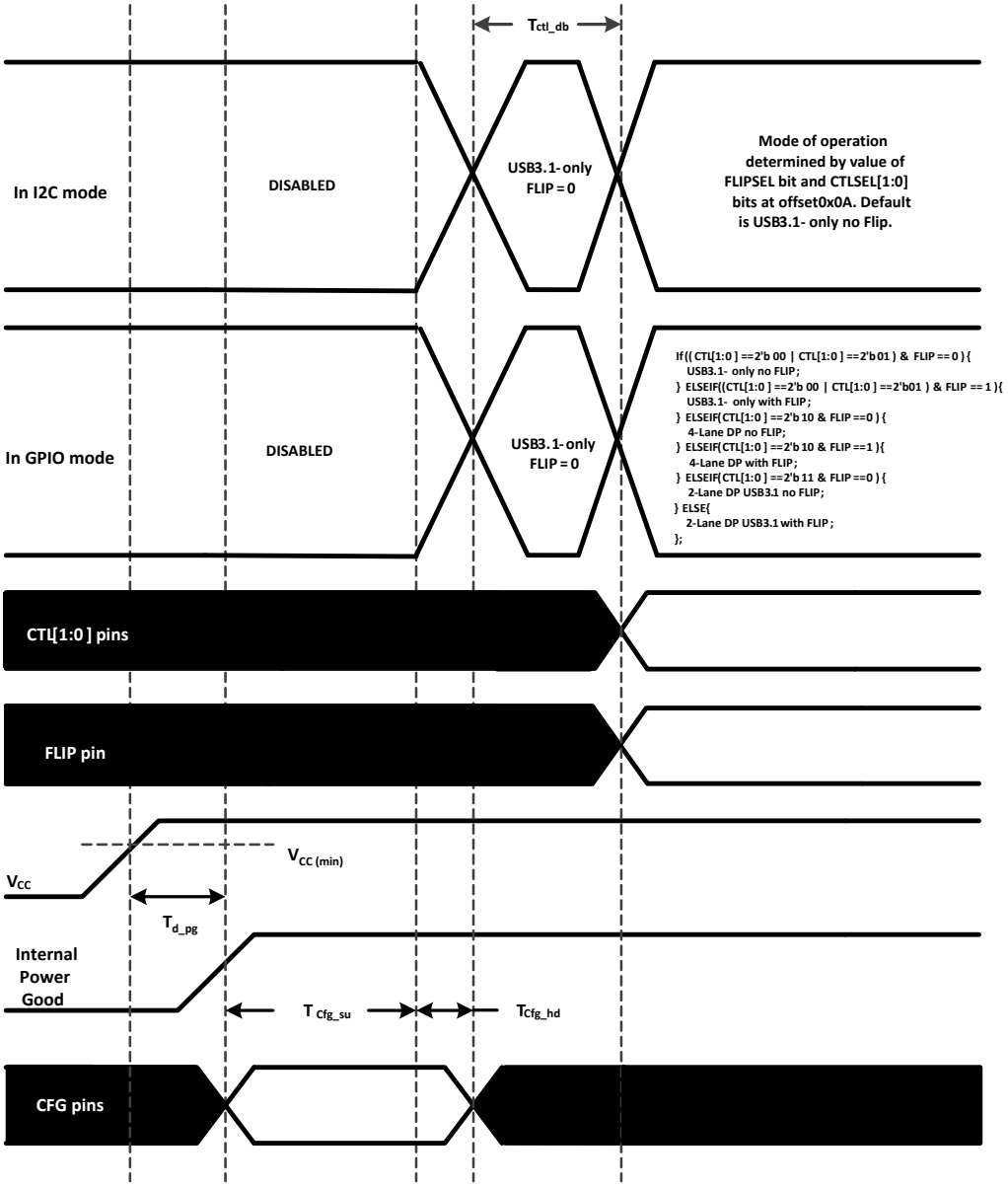


Figure 17. Power-Up Timing

Table 8. Power-Up Timing(1)(2)

PARAMETER		MIN	MAX	UNIT
t_{d_pg}	V_{CC} (minimum) to Internal Power Good asserted high		500	µs
t_{cfg_su}	CFG(1) pins setup(2)	50		µs
t_{cfg_hd}	CFG(1) pins hold	10		µs
t_{CTL_DB}	CTL[1:0] and FLIP pin debounce		16	ms
t_{VCC_RAMP}	VCC supply ramp requirement	0.1	100	ms

(1) Following pins comprise CFG pins: I2C_EN, EQ[1:0], SSEQ[1:0], and DPEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at minimum value.

8.5 Programming

For further programmability, the TUSB564 can be controlled using I^2C. The SCL and SDA pins are used for I^2C clock and I^2C data respectively.

Table 9. TUSB564 I^2C Target Address

DPEQ0/A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

The following procedure should be followed to write to TUSB564 I^2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB564 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB564 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within TUSB564) to be written, consisting of one byte of data, MSB-first.
4. The TUSB564 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^2C register.
6. The TUSB564 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB564.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TUSB564 I^2C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB564 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TUSB564 acknowledges the address cycle.
3. The TUSB564 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the I^2C register occurred prior to the read, then the TUSB564 shall start at the sub-address specified in the write.
4. The TUSB564 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^2C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TUSB564 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I^2C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB564 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB564 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within TUSB564) to be written, consisting of one byte of data, MSB-first.

4. The TUSB564 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

NOTE

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I^2C master terminates the read operation. If a I^2C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

Table 10. Register Legend

ACCESS TAG	NAME	MEANING
R	Read	The field may be read by software
W	Write	The field may be written by software
S	Set	The field may be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable

8.6 Register Maps

8.6.1 General Register (address = 0x0A) [reset = 00000001]

Figure 18. General Registers

7	6	5	4	3	2	1	0
Reserved		Reserved	EQ_OVERRIDE	HPDIN_OVRRIDE	FLIPSEL	CTLSEL[1:0].	
R		R	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. General Registers

Bit	Field	Type	Reset	Description
7:5	Reserved.	R	00	Reserved.
4	EQ_OVERRIDE	R/W	0	Setting of this field will allow software to use EQ settings from registers instead of value sample from pins. 0 – EQ settings based on sampled state of the EQ pins (SSEQ[1:0], EQ[1:0], and DPEQ[1:0]). 1 – EQ settings based on programmed value of each of the EQ registers
3	DP_EN_CTRL	R/W	0	Controls whether DisplayPort functionality is controlled by CTLSEL1 register or CTL1 pin. 0 – DisplayPort enable/disable is based on CTLSEL1 register. 1 – DisplayPort enable/disable is based on state of CTL1 pin.
2	FLIPSEL	R/W	0	FLIPSEL. Refer to Table 5 and Table 6 for this field functionality.
1:0	CTLSEL[1:0].	R/W	01	00 – Disabled. All RX and TX for USB3 and DisplayPort are disabled. 01 – USB3.1 only enabled. (Default) 10 – Four DisplayPort lanes enabled. 11 – Two DisplayPort lanes and one USB3.1

8.6.2 DisplayPort Control/Status Registers (address = 0x10) [reset = 00000000]

Figure 19. DisplayPort Control/Status Registers (0x10)

7	6	5	4	3	2	1	0
DP1EQ_SEL				DP3EQ_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. DisplayPort Control/Status Registers (0x10)

Bit	Field	Type	Reset	Description
7:4	DP1EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 1. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 1 based on value written to this field.
3:0	DP3EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 3. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 3 based on value written to this field.

8.6.3 DisplayPort Control/Status Registers (address = 0x11) [reset = 00000000]

Figure 20. DisplayPort Control/Status Registers (0x11)

7	6	5	4	3	2	1	0
DP0EQ_SEL				DP2EQ_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. DisplayPort Control/Status Registers (0x11)

Bit	Field	Type	Reset	Description
7:4	DP0EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 0. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 0 based on value written to this field.
3:0	DP2EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 2. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 2 based on value written to this field.

8.6.4 DisplayPort Control/Status Registers (address = 0x12) [reset = 00000000]

Figure 21. DisplayPort Control/Status Registers (0x12)

7	6	5	4	3	2	1	0
Reserved	SET_POWER_STATE			LANE_COUNT_SET			
R	RU			RU			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. DisplayPort Control/Status Registers (0x12)

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6:5	SET_POWER_STATE	R/U	00	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 1'b0, the TUSB564 will enable/disable DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1'b1, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 2'b00 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.
4:0	LANE_COUNT_SET	R/U	00000	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 1'b0, TUSB564 will enable DP lanes specified by the snoop value. Unused DP lanes will be disabled to save power. When AUX_SNOOP_DISABLE = 1'b1, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0x0 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.

8.6.5 DisplayPort Control/Status Registers (address = 0x13) [reset = 00000000]

Figure 22. DisplayPort Control/Status Registers (0x13)

7	6	5	4	3	2	1	0
AUX_SNOOP_DISABLE	Reserved	AUX_SBU_OVR		DP3_DISABLE	DP2_DISABLE	DP1_DISABLE	DP0_DISABLE
R/W	R	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. DisplayPort Control/Status Registers (0x13)

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0	0 – AUX snoop enabled. (Default) 1 – AUX snoop disabled.
6	Reserved	R	0	Reserved
5:4	AUX_SBU_OVR	R/W	00	This field overrides the AUXp or AUXn to SBU1 or SBU2 connect and disconnect based on CTL1 and FLIP. Changing this field to 2'b01 or 2'b10 will allow traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register 00 – AUX to SBU connect/disconnect determined by CTLSEL1 and FLIPSEL (Default) 01 – AUXn -> SBU1 and AUXp -> SBU2 connection always enabled. 10 – AUXn -> SBU2 and AUXp -> SBU1 connection always enabled. 11 – AUX to SBU open.
3	DP3_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 3 functionality. 0 – DP Lane 3 Enabled (default) 1 – DP Lane 3 Disabled.
2	DP2_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 2 functionality. 0 – DP Lane 2 Enabled (default) 1 – DP Lane 2 Disabled.
1	DP1_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 1 functionality. 0 – DP Lane 1 Enabled (default) 1 – DP Lane 1 Disabled.
0	DP0_DISABLE	R/W	0	DISABLE. When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 0 functionality. 0 – DP Lane 0 Enabled (default) 1 – DP Lane 0 Disabled.

8.6.6 USB3.1 Control/Status Registers (address = 0x20) [reset = 00000000]

Figure 23. USB3.1 Control/Status Registers (0x20)

7	6	5	4	3	2	1	0
EQ2_SEL				EQ1_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. USB3.1 Control/Status Registers (0x20)

Bit	Field	Type	Reset	Description
7:4	EQ2_SEL	R/W/U	0000	Field selects EQ level for USB3.1 RX2 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX2 receiver based on value written to this field.
3:0	EQ1_SEL	R/W/U	0000	Field selects EQ level for USB3.1 RX1 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX1 receiver based on value written to this field.

8.6.7 USB3.1 Control/Status Registers (address = 0x21) [reset = 00000000]

Figure 24. USB3.1 Control/Status Registers (0x21)

7	6	5	4	3	2	1	0
Reserved				SSEQ_SEL			
R				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. USB3.1 Control/Status Registers (0x21)

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0000	Reserved
3:0	SSEQ_SEL	R/W/U	0000	Field selects between 0 to 11 dB of EQ for USB3.1 SSTXP/N receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 SSTXP/N receiver based on value written to this field.

8.6.8 USB3.1 Control/Status Registers (address = 0x22) [reset = 00000000]

Figure 25. USB3.1 Control/Status Registers (0x22)

7	6	5	4	3	2	1	0
CM_ACTIVE	LFPS_EQ	U2U3_LFPS_DEBOUNCE	DISABLE_U2U3_RXDET	DFP_RXDET_INTERVAL		USB3_COMPLIANCE_CTRL	
R/U	R/W	R/W	R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. USB3.1 Control/Status Registers (0x22)

Bit	Field	Type	Reset	Description
7	CM_ACTIVE	R/U	0	0 –device not in USB 3.1 compliance mode. (Default) 1 –device in USB 3.1 compliance mode
6	LFPS_EQ	R/W	0	Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL and SSEQ_SEL applies to received LFPS signal. 0 – EQ set to zero when receiving LFPS (default) 1 – EQ set to EQ1_SEL, EQ2_SEL, and SSEQ_SEL when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0	0 – No debounce of LFPS before U2/U3 exit. (Default) 1 – 200us debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0	0 – Rx.Detect in U2/U3 enabled. (Default) 1 – Rx.Detect in U2/U3 disabled.
3:2	DFP_RXDET_INTERVAL	R/W	00	This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N). 00 – 8 ms 01 – 12 ms (default) 10 – Reserved 11 – Reserved
1:0	USB3_COMPLIANCE_CTRL	R/W	00	00 – FSM determined compliance mode. (Default) 01 – Compliance Mode enabled in DFP direction (SSTX -> TX1/TX2) 10 – Compliance Mode enabled in UFP direction (RX1/RX2 -> SSRX) 11 – Compliance Mode Disabled.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TUSB564 is a linear redriver designed specifically to compensation for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB564 has four independent DisplayPort 1.4 inputs, one upstream facing USB 3.1 Gen 1 input, and two downstream facing USB 3.1 Gen 1 inputs, it can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB564 between a USB3.1 Host/DisplayPort 1.4 GPU and a USB3.1 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

9.2 Typical Application

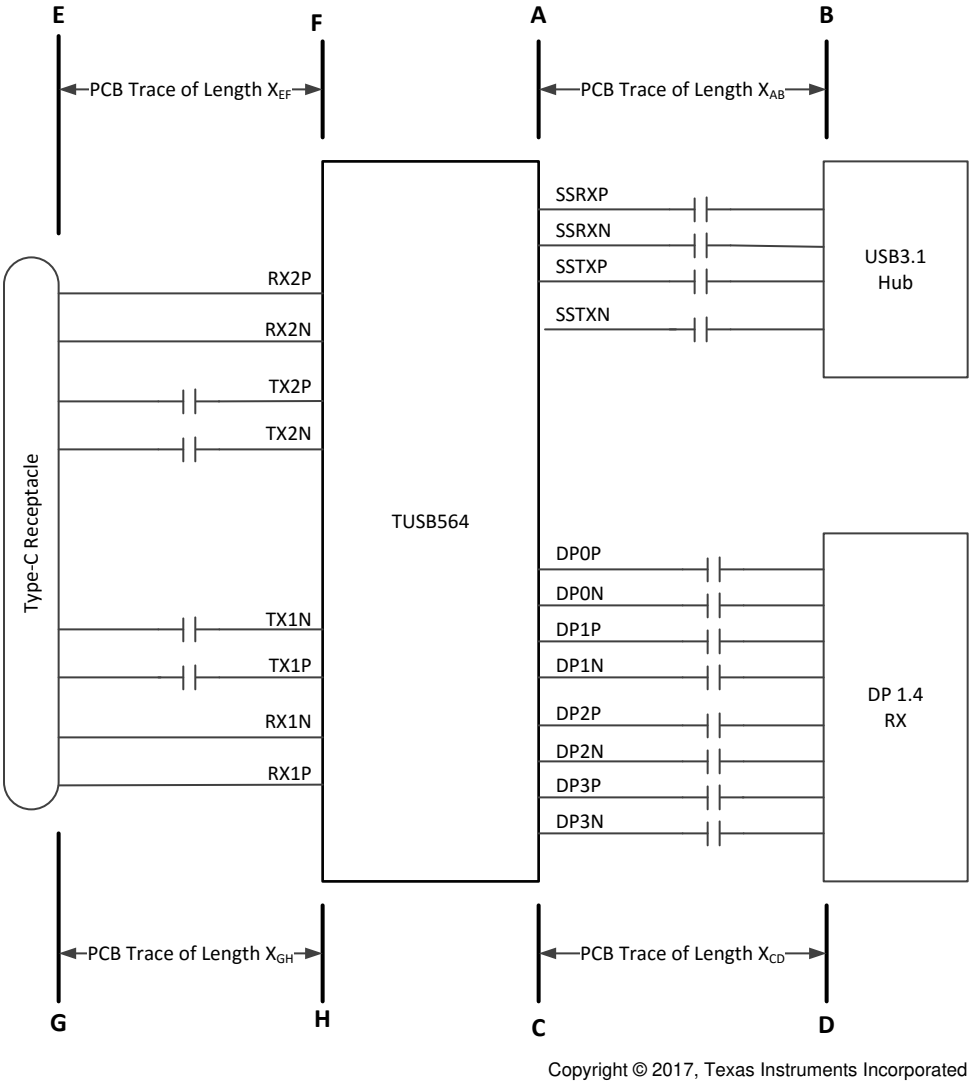


Figure 26. TUSB564 in a Host Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 19.

Table 19. Design Parameters

PARAMETER	VALUE
A to B PCB trace length, X_{AB}	12 inches
C to D PCB trace length, X_{CD}	12 inches
E to F PCB trace length, X_{EF}	2 inches
G to H PCB trace length, X_{GH}	2 inches
PCB trace width	4 mils
AC-coupling capacitor (75 nF to 265 nF)	100 nF
VCC supply (3 V to 3.6 V)	3.3 V
I2C Mode or GPIO Mode	I2C Mode. (I2C_EN pin != "0")
1.8V or 3.3V I2C Interface	3.3V I2C. Pull-up the I2C_EN pin to 3.3V with a 1K ohm resistor. CTL1, EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pin unconnected.
EQ setting for DisplayPort Lanes	EQ Setting # 5 (Register 0x0A[4] = 1'b1, 0x10 = 0x55; 0x11 = 0x55)
EQ setting for Downstream USB Data Path	EQ Setting # 6 (Register 0x0A[4] = 1'b1, 0x20 = 0x66)
EQ setting for Upstream USB Data Path	EQ Setting # 6 (Register 0x0A[4] = 1'b1, 0x21 = 0x08)

9.2.2 Detailed Design Procedure

A typical usage of the TUSB564 device is shown in Figure 27. The device can be controlled either through its GPIO pins or through its I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. In I2C mode, the equalization settings for each receiver can be independently controlled through I2C registers. For this reason, the configuration pin CTL1 and all of the equalization pins (EQ[1:0], SSEQ[1:0], and DPEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB564 7-bit I2C slave address will be 0x12 because both DPEQ/A1 and SSEQ0/A0 will be at pin level "F". If a different I2C slave address is desired, DPEQ/A1 and SSEQ0/A0 pins should be set to a level which produces the desired I2C slave address.

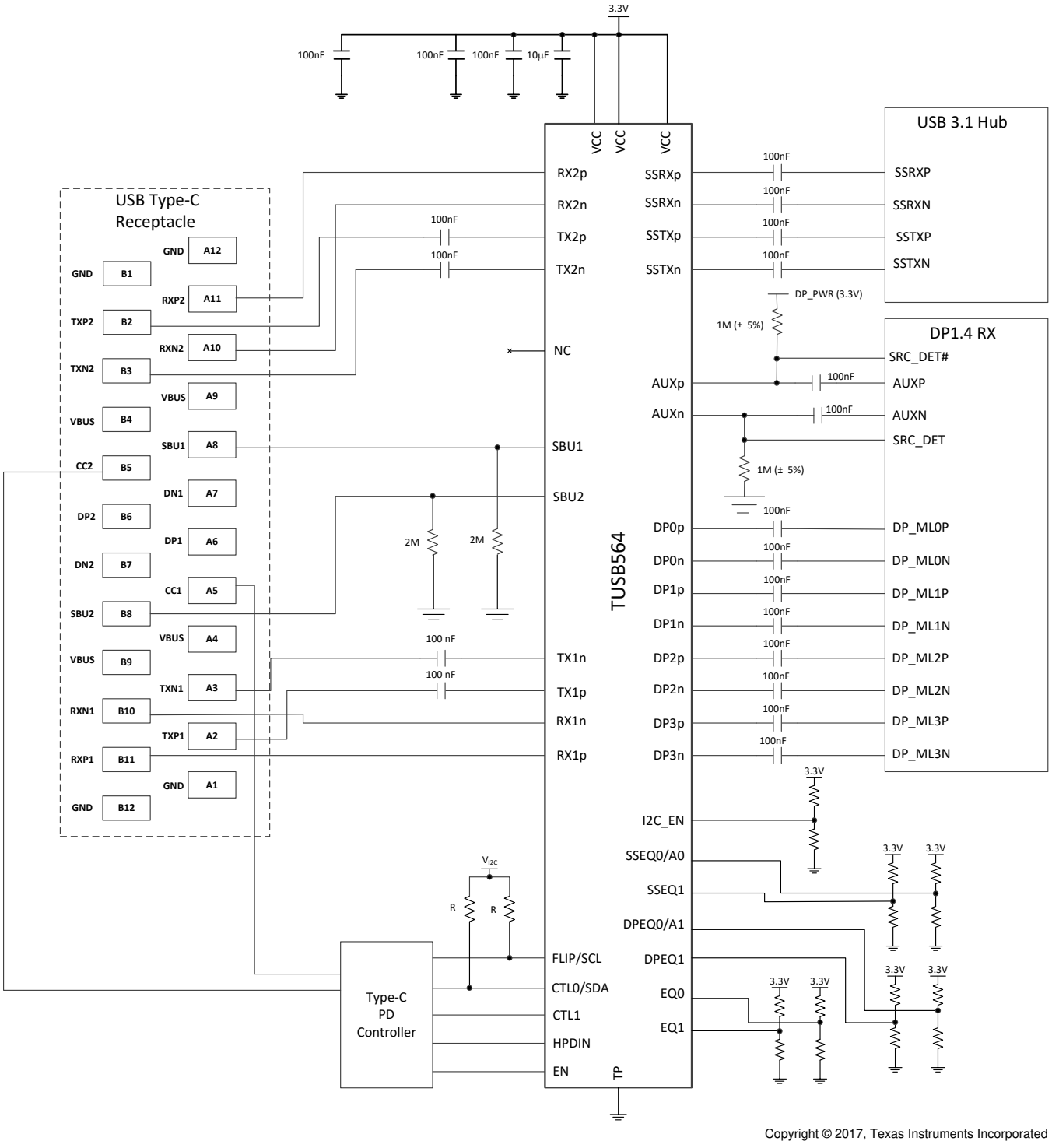


Figure 27. Application Circuit

9.2.3 Support for DisplayPort UFP_D Pin Assignment E

The TUSB564 device can be used in a system that handles DisplayPort UFP_D Pin Assignment E use-case if special measures are taken as described below. With UFP_D Pin Assignment E, the polarity of both the main link and AUX signals is inverted on the Type-C receptacle pins relative to Pin Assignment C. Moreover, on the Type-C receptacle, the location of Lane 0 is swapped with Lane 1 and that of Lane 2 is swapped with Lane 3 relative to Pin Assignment C. For correct reception of the DisplayPort video signal, the system has to comprehend the above-described signaling variation.

The use of the TUSB564 device in a system that handles Pin Assignment E depends on whether AUX-to-SBU switching of the DisplayPort AUX signal is performed internally by the TUSB564 or by external devices such as a PD controller. It also depends on the configuration mode used: I^2C Mode or GPIO Mode. In all those scenarios the TUSB564 passes the polarity of the Main Link signals as received. The DisplayPort sink has to handle the polarity inversion of those signals. Moreover, the DisplayPort sink has to handle the lane swapping with the following lane-to-pin mapping as received by the TUSB564 device: Lane 0 → DP1, Lane 1 → DP0, Lane 2 → DP3, and Lane 3 → DP2.

The use-case with the AUX-to-SBU switching performed internally by the TUSB564 device is shown in Figure 28. If the TUSB564 device configuration is through the I^2C Mode, AUX snooping has to be disabled by setting AUX_SNOOP_DISABLE register 0x13[7] = 1'b1, and manual AUX-to-SBU switching has to be performed through the AUX_SBU_OVR register 0x13[5:4]: AUX_SBU_OVR = 2'b01 for normal USB Type-C plug orientation, or AUX_SBU_OVR = 2'b10 for flipped USB Type-C plug orientation when Pin Assignment E signals are received. If the TUSB564 device configuration is through the GPIO Mode, all 4 DisplayPort lanes are automatically activated. The DisplayPort sink device has to handle the polarity inversion of both the AUX and Main Link signals as well as main link lane swapping.

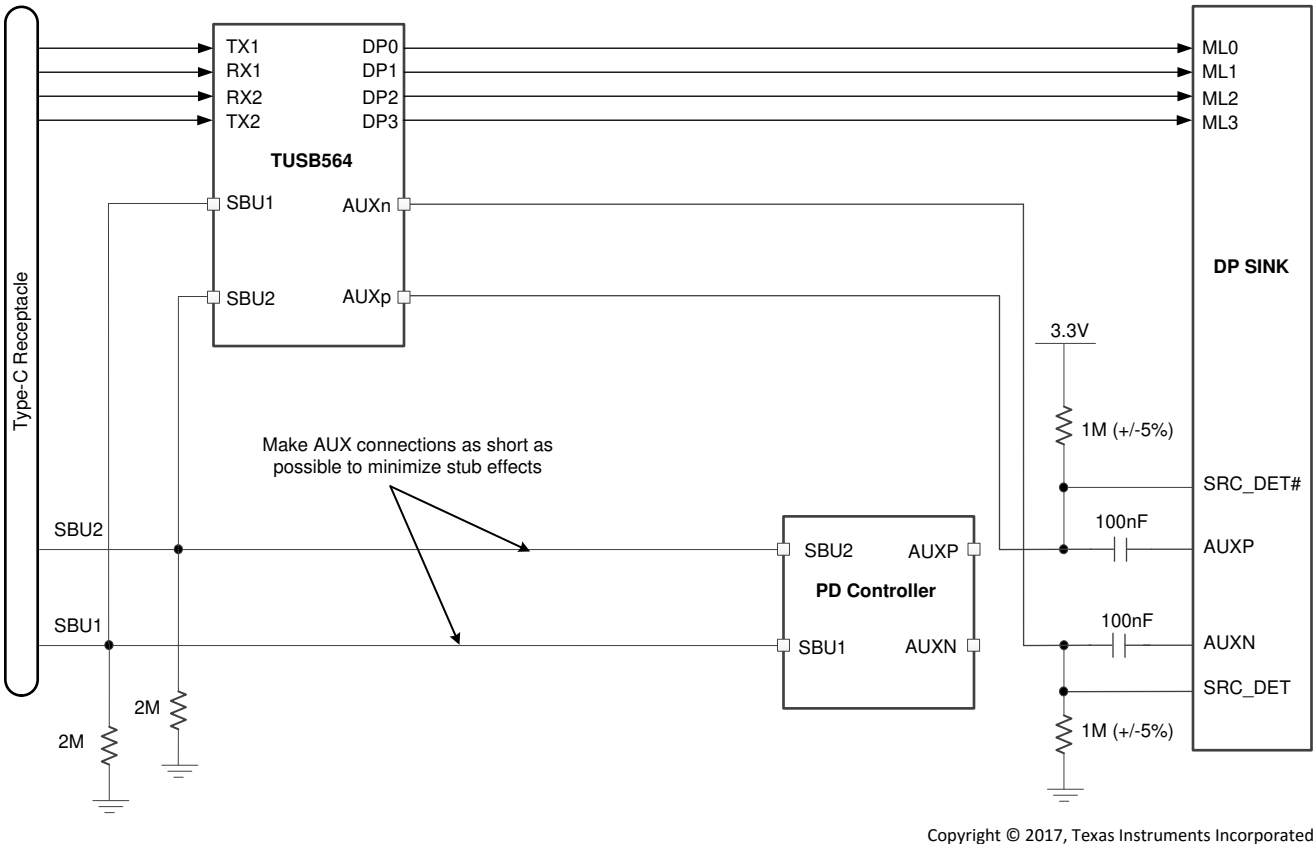


Figure 28. DisplayPort AUX Connections for UFP_D Pin Assignment E with Internal AUX Switching

The use-case with the AUX-to-SBU switching performed by an external device is shown in Figure 29. In this case, it is assumed that the PD controller is capable of correcting the polarity inversion of the AUX signal and the TUSB564 is provided with the corrected polarity of the AUX signal through its AUXp/AUXn pins. If the TUSB564 device configuration is through the I^2C Mode, AUX snooping should be disabled by setting AUX_SNOOP_DISABLE register 0x13[7] = 1'b1. The DisplayPort sink device has to handle the polarity inversion of the Main Link signals as well as the Main Link lane swapping.

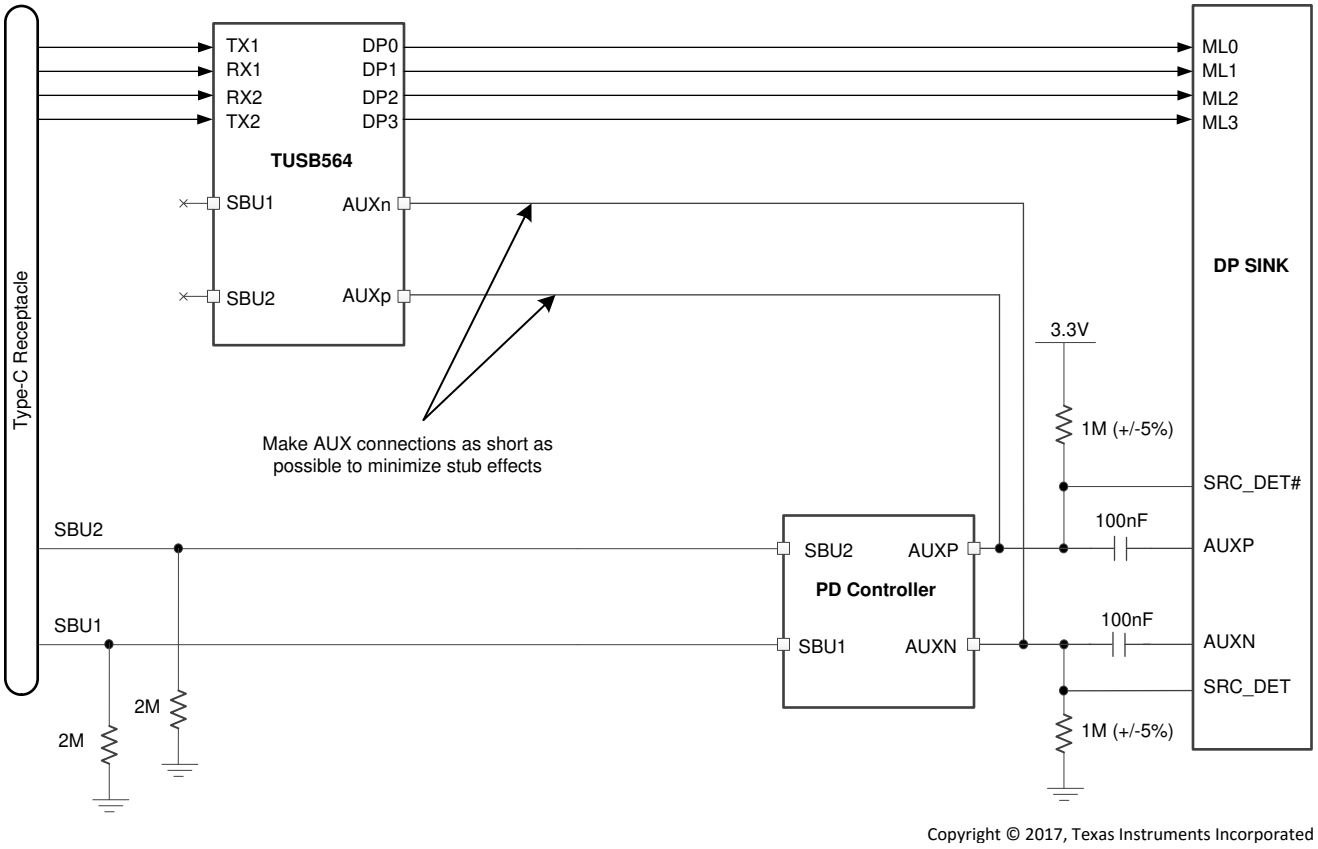


Figure 29. DisplayPort AUX Connections for UFP_D Pin Assignment E with External AUX Switching

9.2.4 PCB Insertion Loss Curves

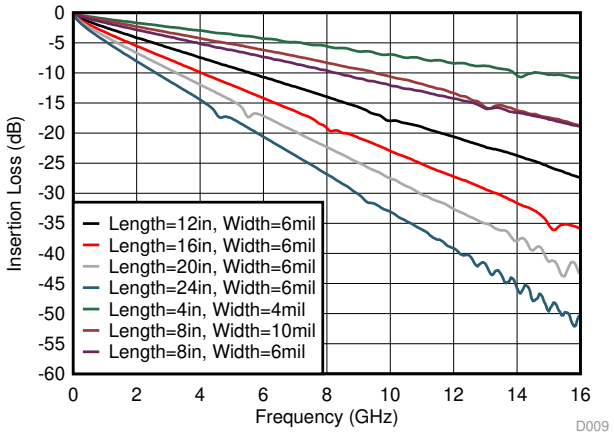


Figure 30. Insertion Loss of FR4 PCB Traces

9.3 System Examples

9.3.1 USB 3.1 Only

The TUSB564 is in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.

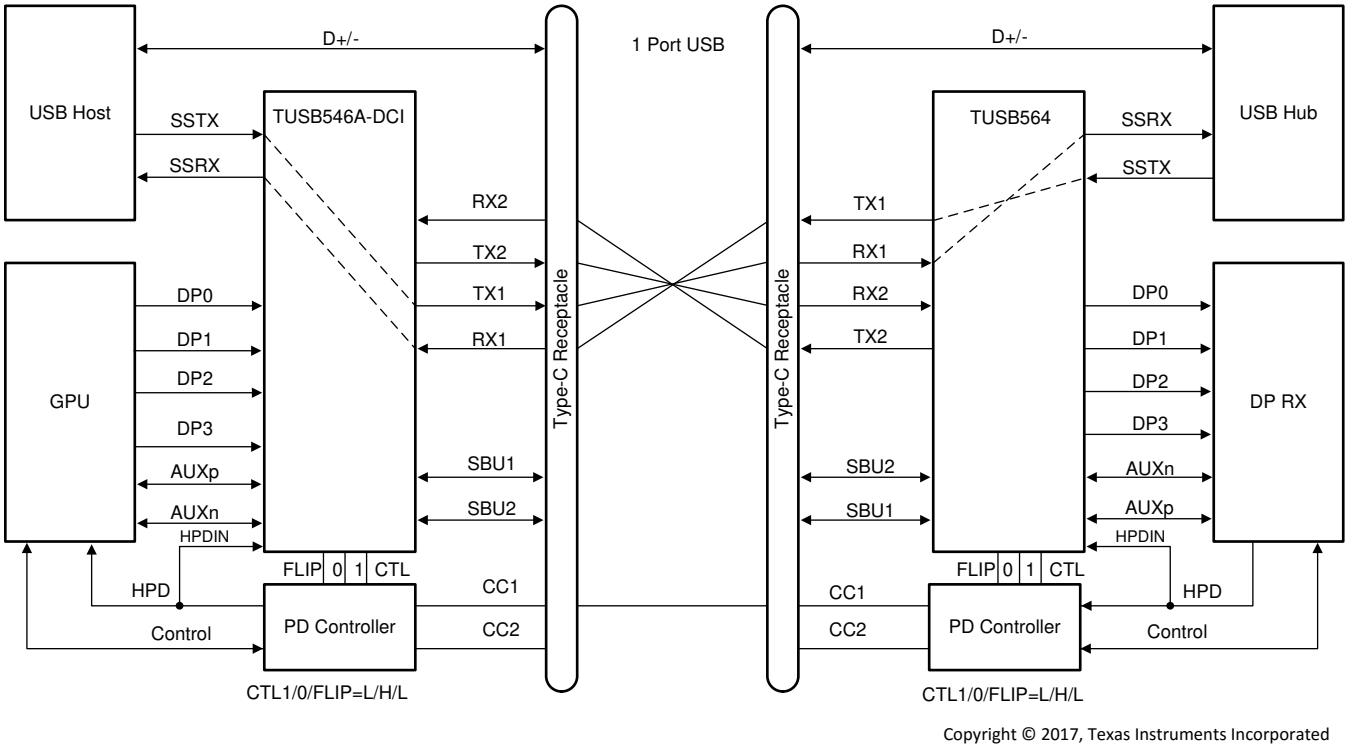


Figure 31. USB3.1 Only – No Flip (CTL1 = L, CTL0 = H, FLIP = L)

System Examples (continued)

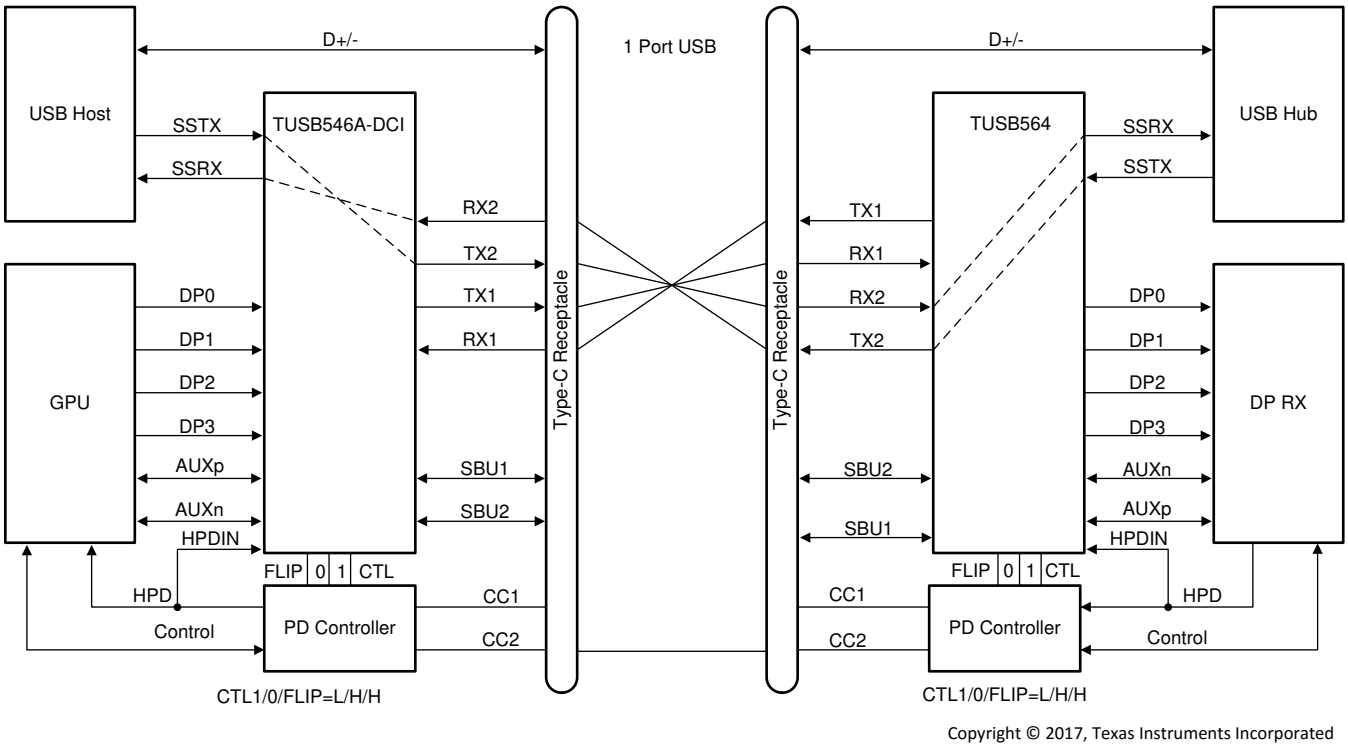


Figure 32. USB3.1 Only – With Flip (CTL1 = L, CTL0 = H, FLIP = H)

System Examples (continued)

9.3.2 USB 3.1 and 2 Lanes of DisplayPort

The TUSB564 operates in USB3.1 and 2 Lanes of DisplayPort mode when the CTL1 pin is high and CTL0 pin is high.

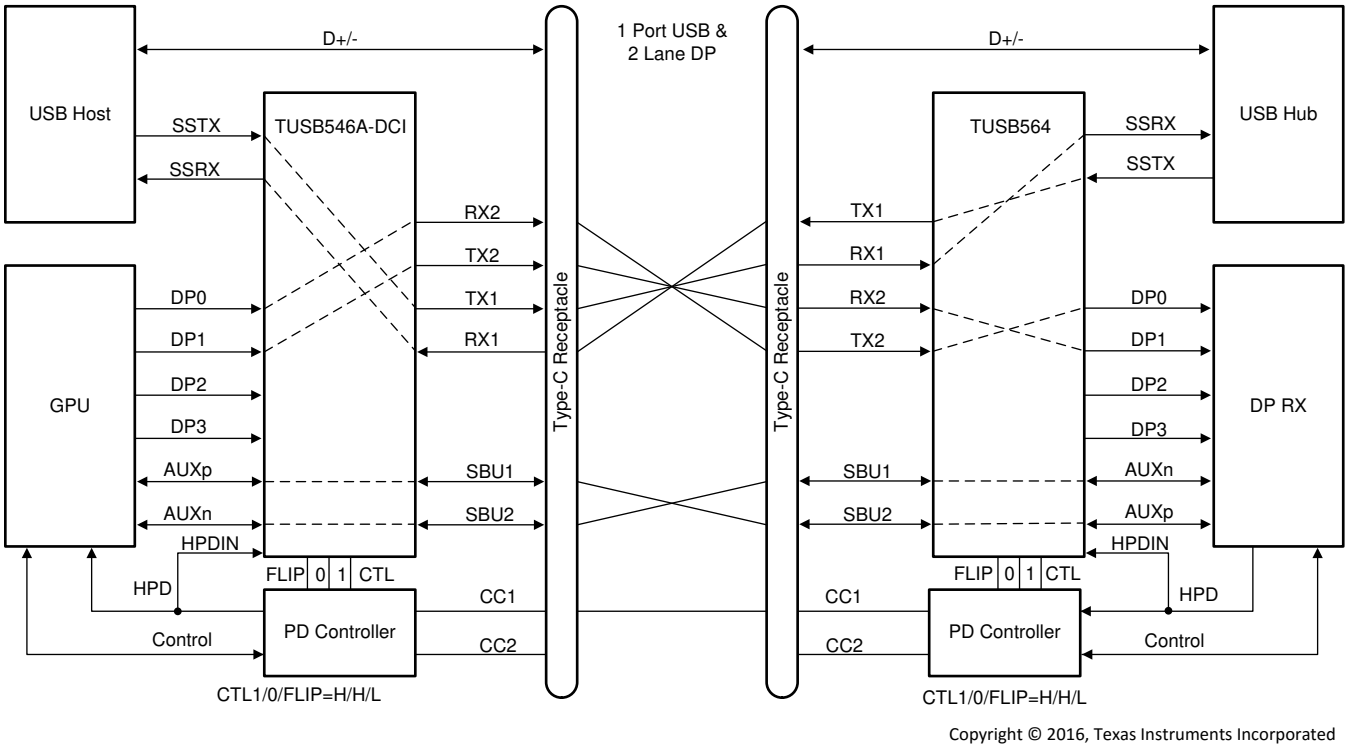


Figure 33. USB3.1 + 2 Lane DP – No Flip (CTL1 = H, CTL0 = H, FLIP = L)

System Examples (continued)

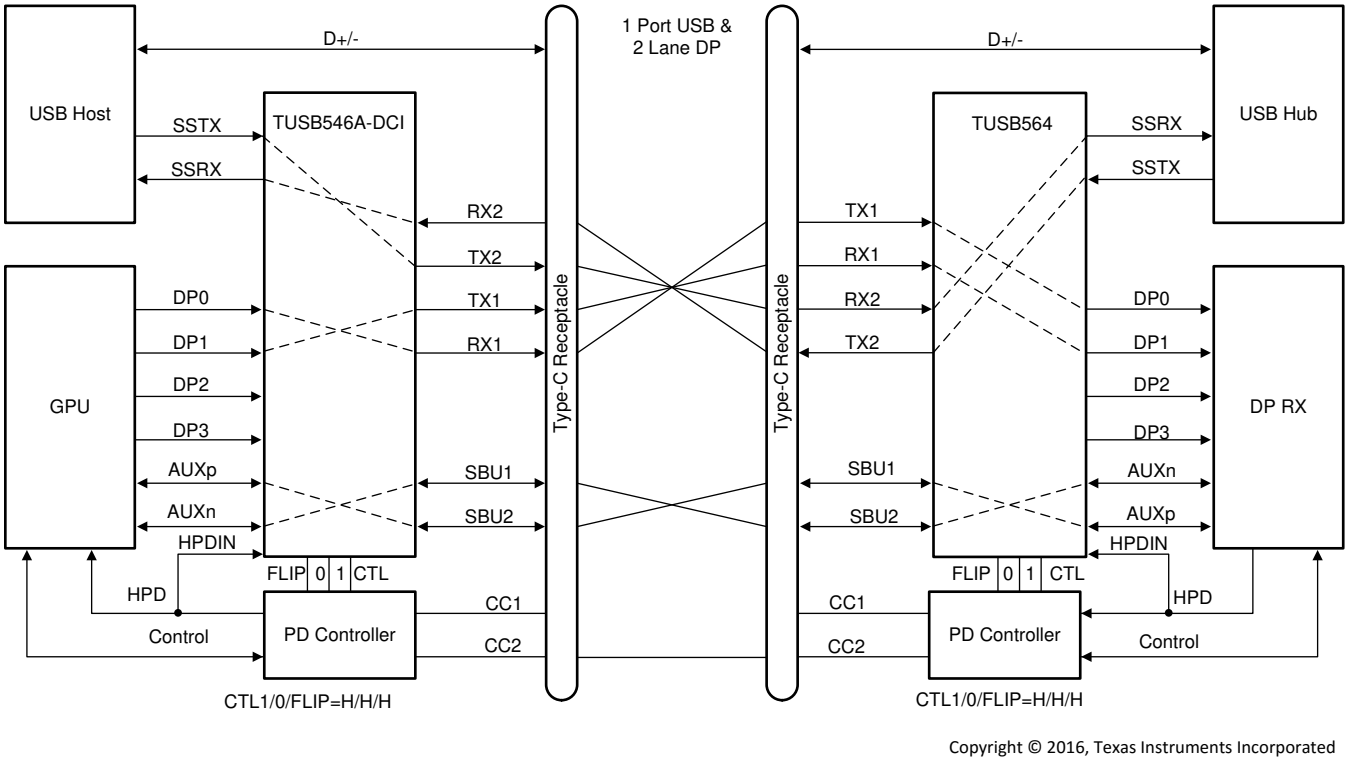


Figure 34. USB 3.1 + 2 Lane DP – Flip (CTL1 = H, CTL0 = H, FLIP = H)

System Examples (continued)

9.3.3 DisplayPort Only

The TUSB564 operates in 4 Lanes of DisplayPort only mode when the CTL1 pin is high and CTL0 pin is low.

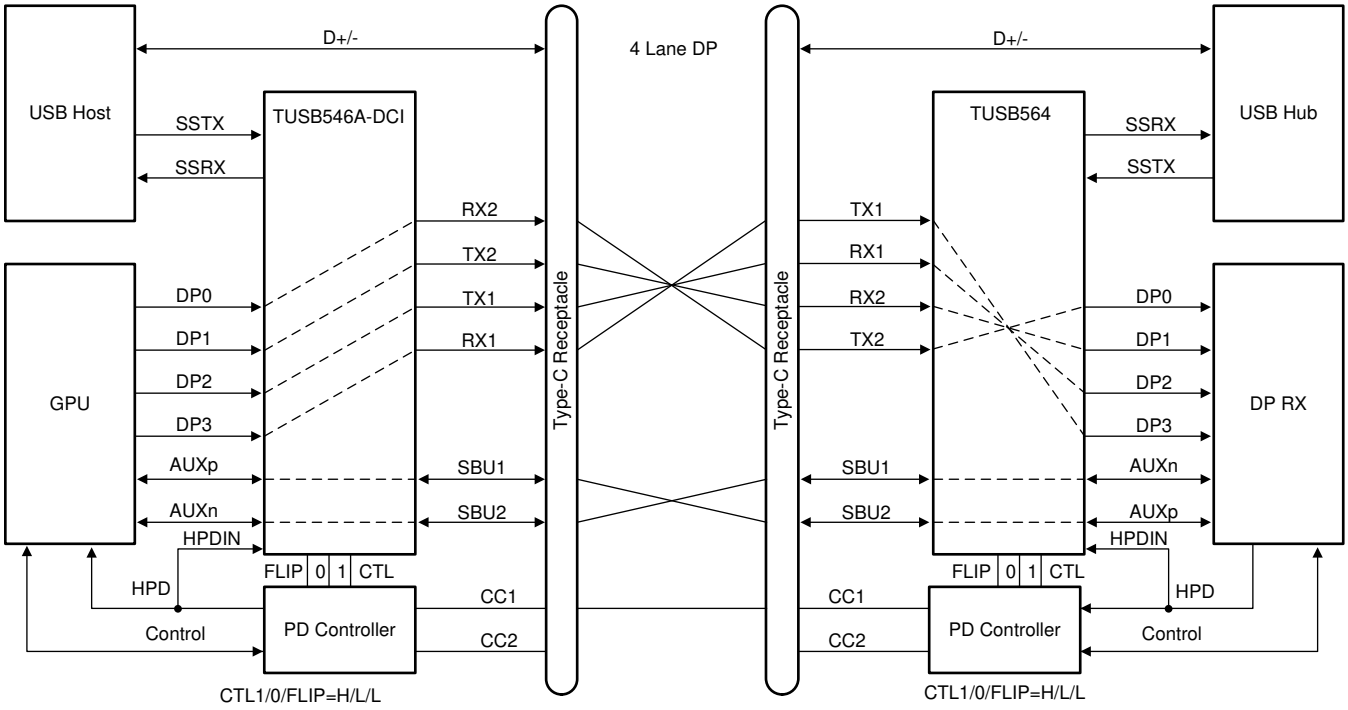


Figure 35. Four Lane DP – No Flip (CTL1 = H, CTL0 = L, FLIP = L)

System Examples (continued)

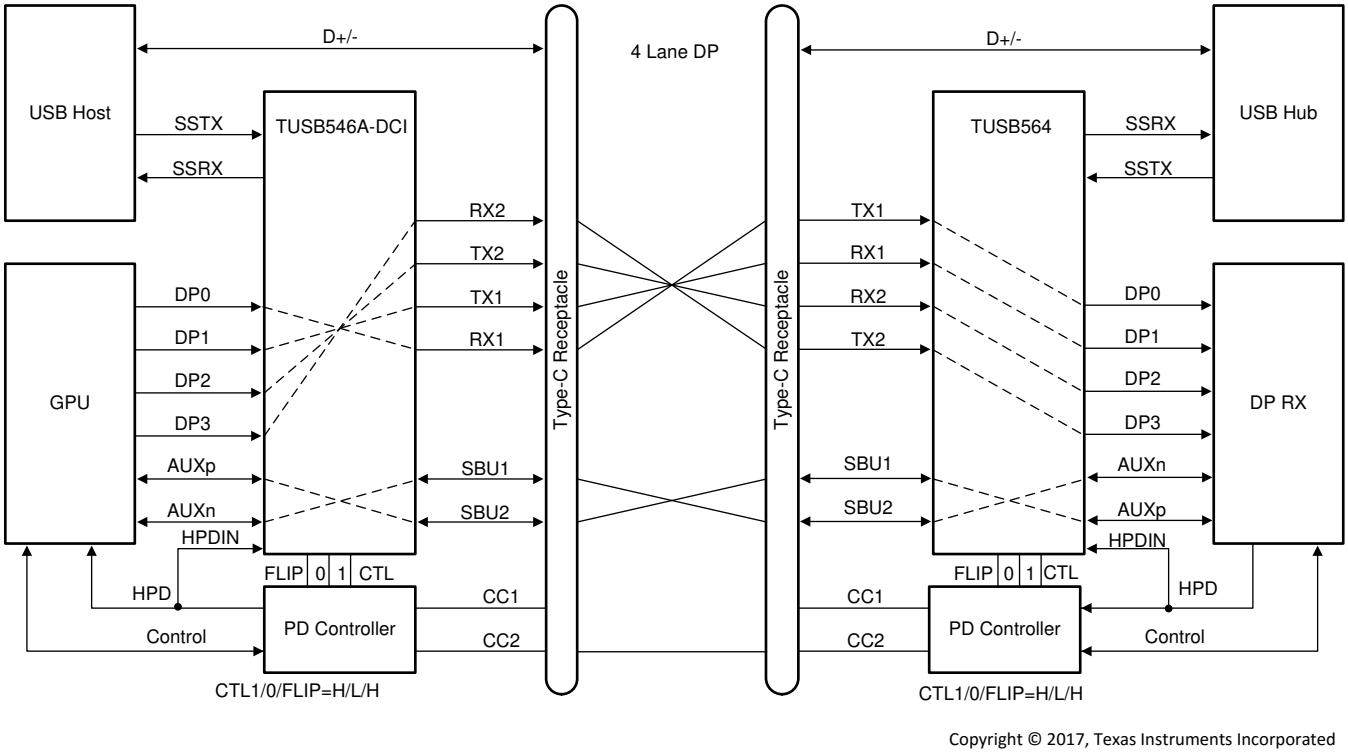


Figure 36. Four Lane DP – With Flip (CTL1 = H, CTL0 = L, FLIP = H)

10 Power Supply Recommendations

The TUSB564 is designed to operate with a 3.3-V power supply. Levels above those listed in the table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-µF capacitor should be used on each power pin.

11 Layout

11.1 Layout Guidelines

1. RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
2. Keep away from other high speed signals.
3. Intra-pair routing should be kept to within 2 mils.
4. Length matching should be near the location of mismatch.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

11.2 Layout Example

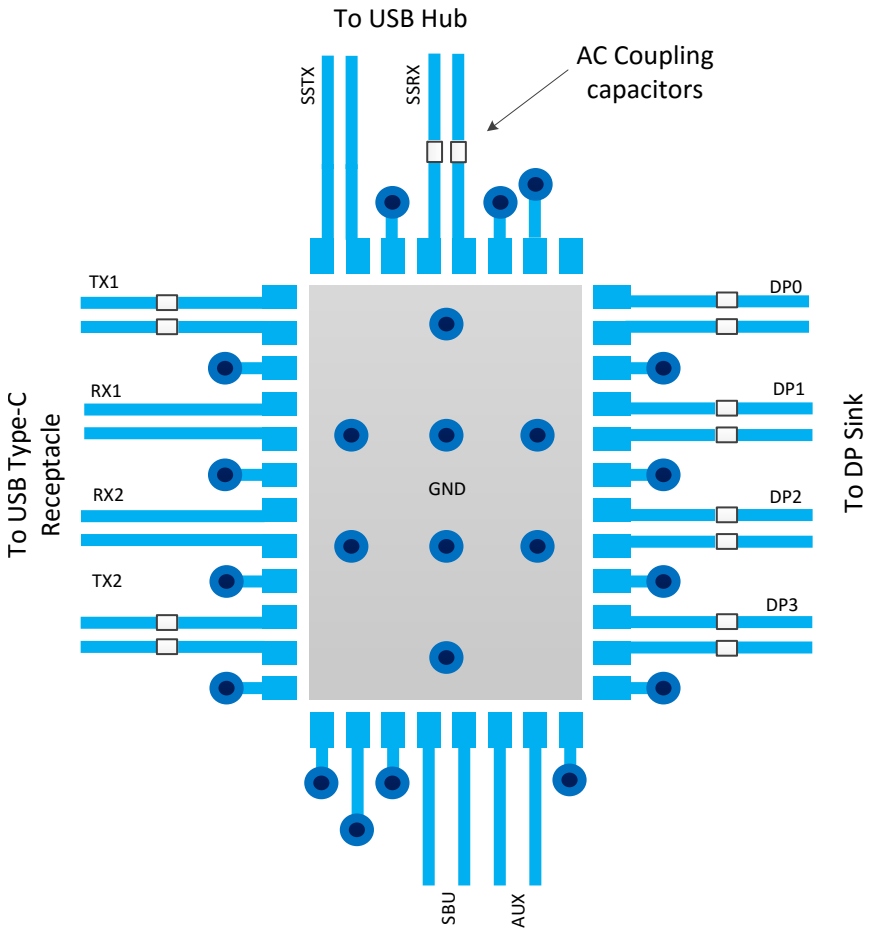


Figure 37. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
DisplayPort is a trademark of VESA.
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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB564IRNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TUSB64	Samples
TUSB564IRNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TUSB64	Samples
TUSB564RNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TUSB64	Samples
TUSB564RNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TUSB64	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

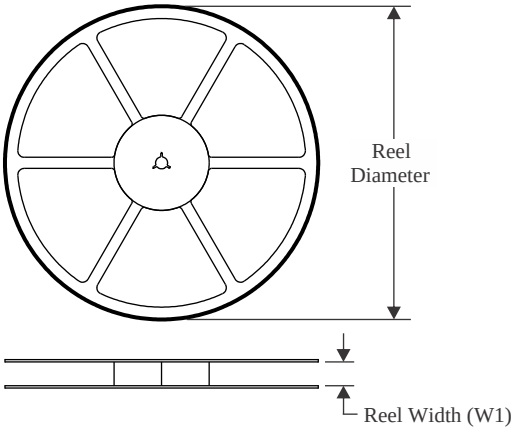
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

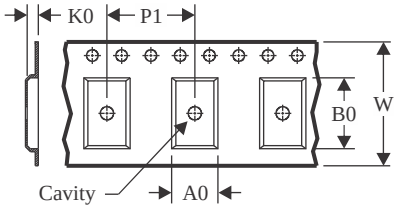
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

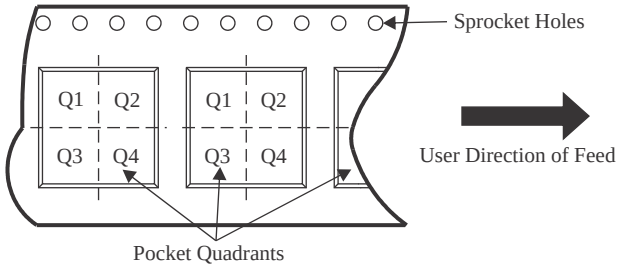


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

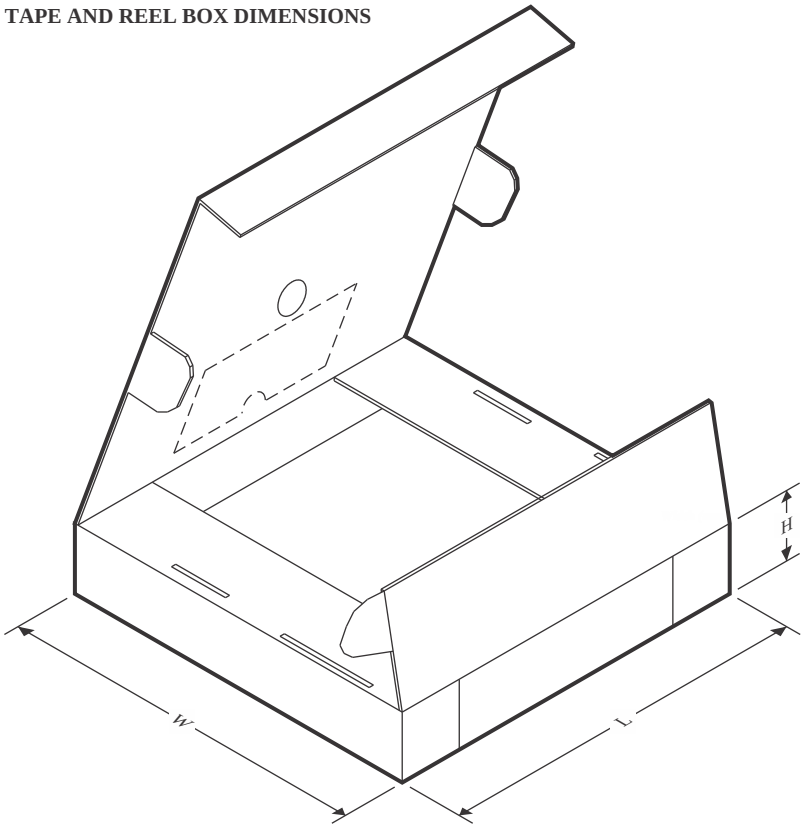
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB564IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB564IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB564RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB564RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

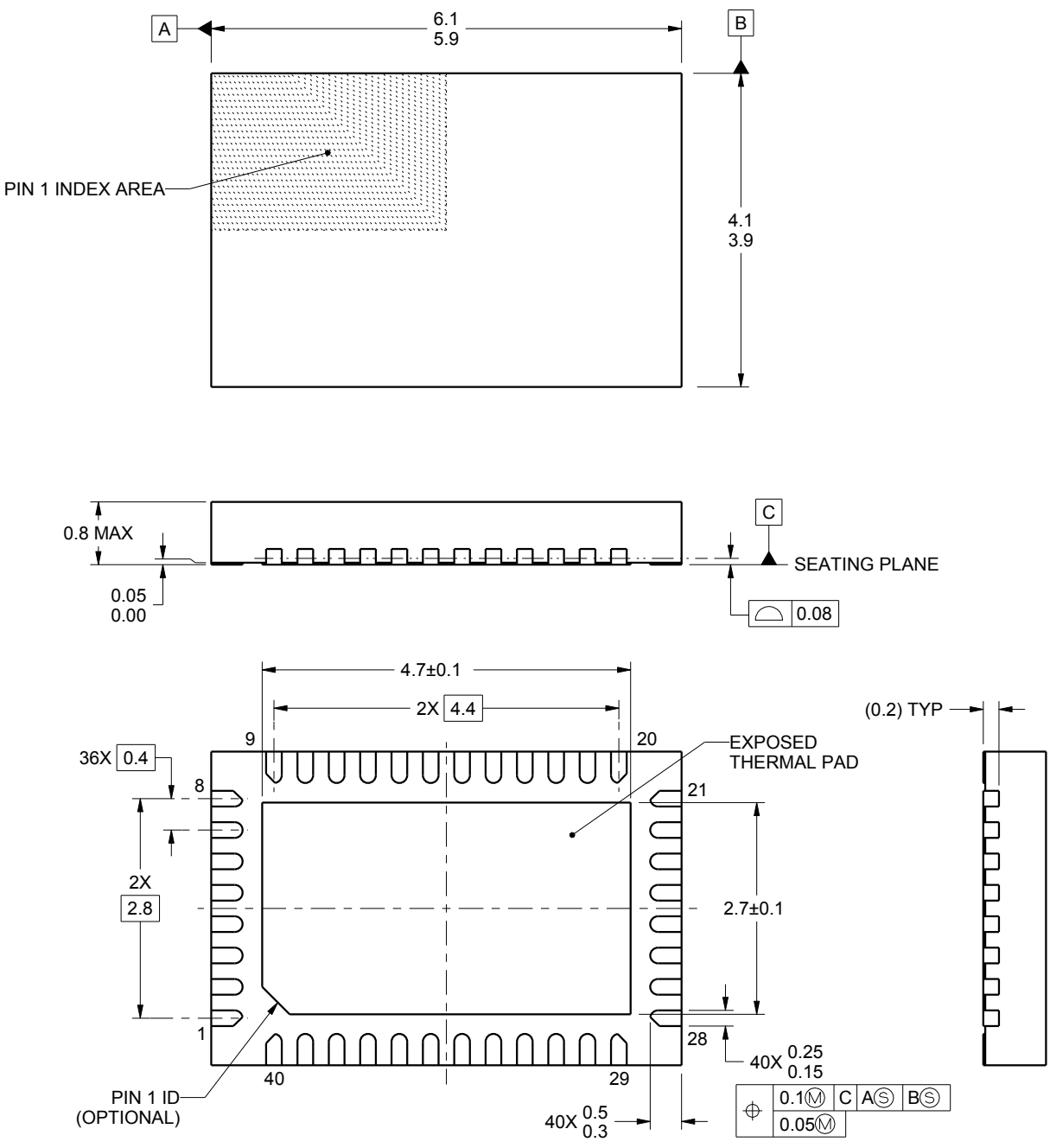
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB564IRNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB564IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0
TUSB564RNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB564RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNQ0040A

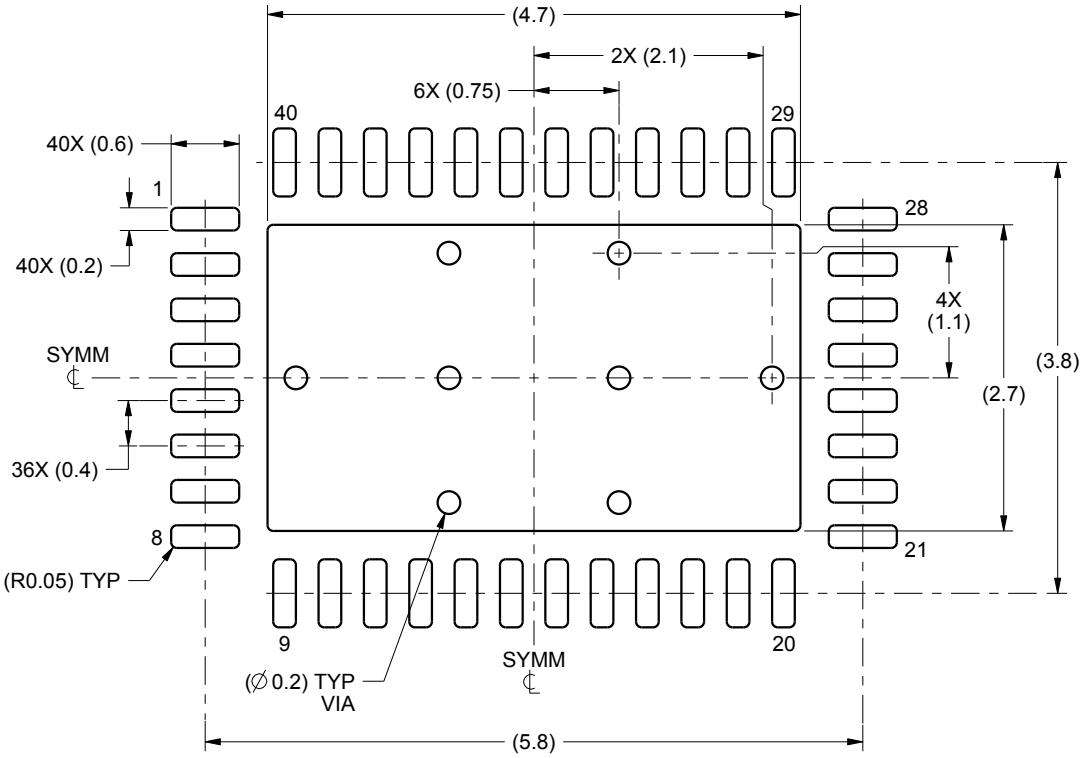
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

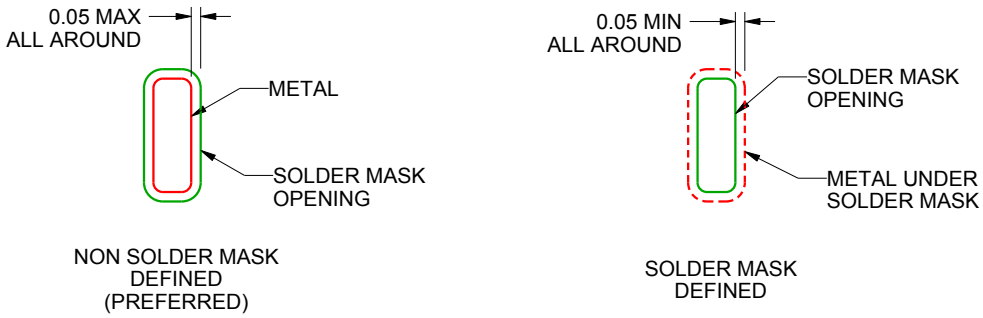


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

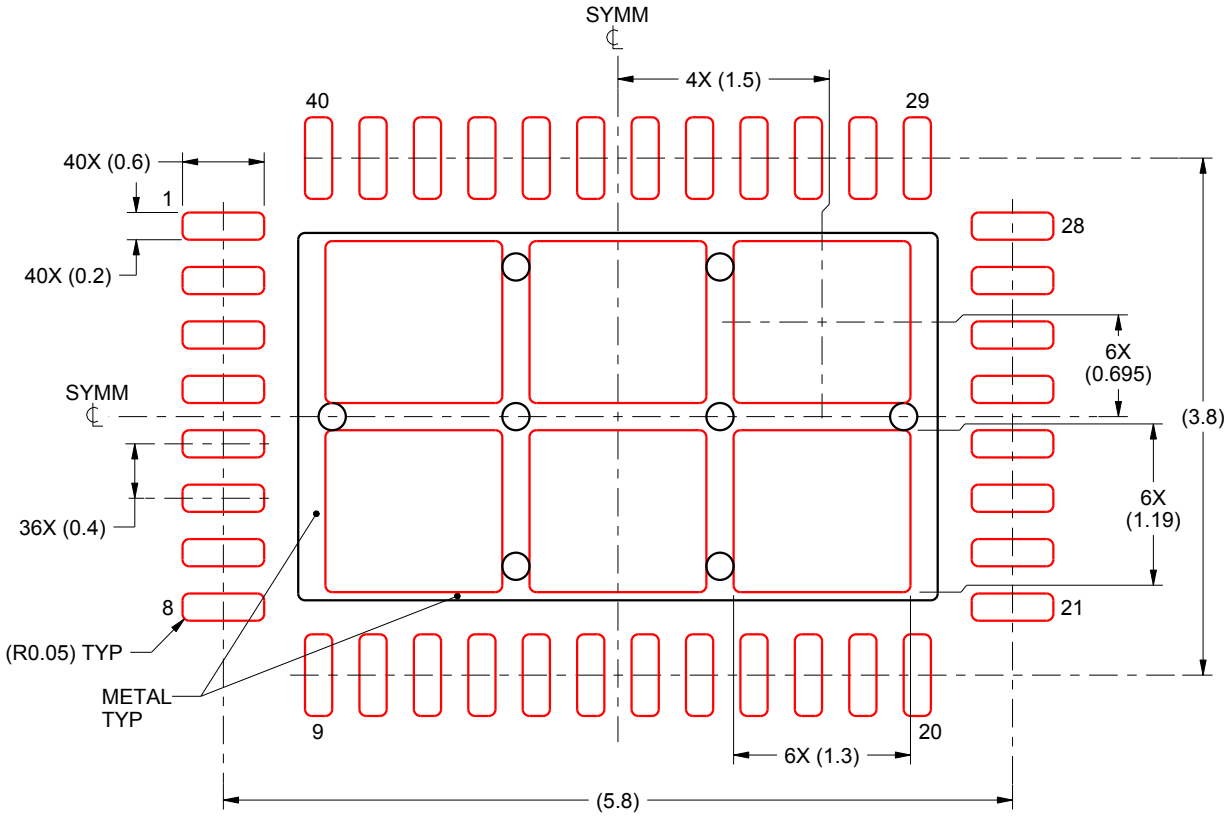


SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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