Features

- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs For Noise Suppression**
- **DDC1™/ DDC2™ Interface Compliant for Monitor Identification**
- **Low-voltage Operation**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
- **Internally Organized 128 x 8**
- **100 kHz (2.5V) Compatibility**
- **8-byte Page Write Mode**
- **Write Protection Available**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
  - **ESD Protection: >3000V**
- **8-pin PDIP and JEDEC SOIC Packages**

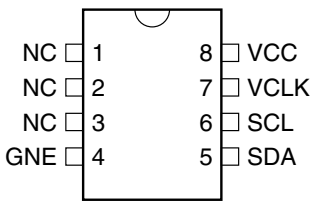
Description

The AT24C21 provides 1024 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128 words of 8 bits each. The device is optimized for use in applications requiring data storage and serial transmission of configuration and control information. The AT24C21 features two modes of operation: Transmit-only Mode and Bidirectional Mode. Upon power-up, the AT24C21 will be in the Transmit-only Mode, sending a serial-bit stream of the entire memory contents, clocked via the VCLK pin. The Bidirectional Mode is selected by a valid high-to-low transition on the SCL pin and offers byte selectable read/write capability of the entire memory array. The AT24C21 is available in space saving 8-pin PDIP and 8-lead SOIC packages.

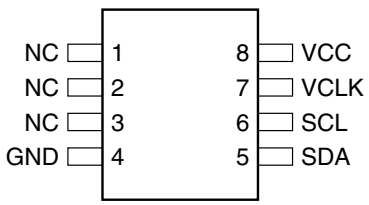
Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input (Bidirectional Mode)
VCLK	Serial Clock Input (Transmit-only Mode)

8-pin PDIP



8-lead SOIC



2-wire Serial EEPROM

1K (128 x 8)

AT24C21

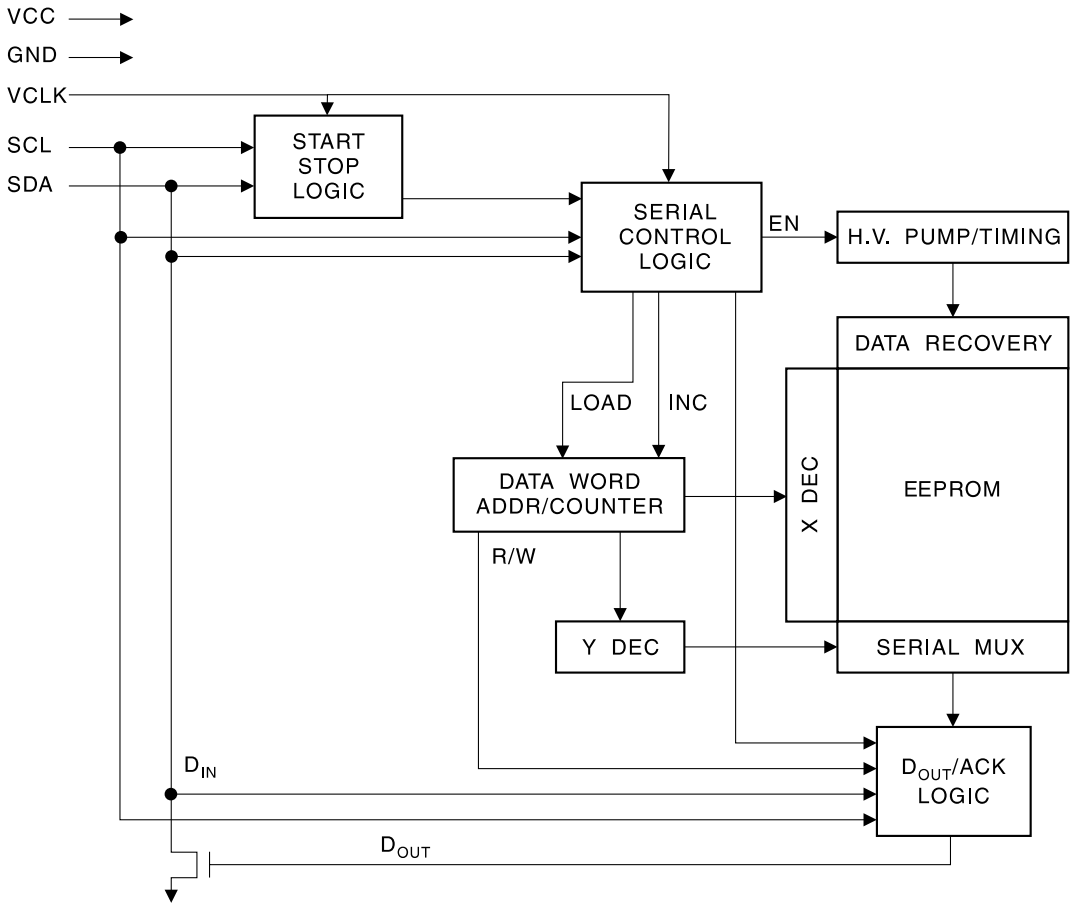
Rev. 0405F–01/00

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices.

SERIAL CLOCK (VCLK): Upon power-up, the device is in the Transmit-only mode and will transmit the entire memory contents via the SDA pin with positive signals on the VCLK pin.

Memory Organization

AT24C21, 1K SERIAL EEPROM: Internally organized with 128 pages of one byte each. The 1K requires a 7-bit data word address for random word addressing.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 KHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 KHz		2.0	3.0	mA
I_{SB}	Standby Current V_{CC} = 2.5V V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS} V_{IN} = V_{CC} or V_{SS}		3.0 12.0	4.0 30.0	µA µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	1.0	µA
V_{IL}	Input Low Level(1) SCL, SDA Pin Input Low Level VCLK Pin	 $V_{CC} \geq 2.7V$ $V_{CC} < 2.7V$	-0.6		$V_{CC} \times 0.3$ 0.8 $0.2 \times V_{CC}$	V V V
V_{IH}	Input High Level(1) SCL, SDA Pin Input High Level VCLK Pin		$V_{CC} \times 0.7$ 2.0		V_{CC} + 0.5	V V
V_{OL}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.40	V

Note: 1. V_{IL} min and V_{IH} max are for reference only and not tested.

Pin Capacitance(1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL, VCLK)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Transmit-only Mode

		2.5-volt		
Symbol	Parameter	Min	Max	Units
T_{VAA}	Output valid from VCLK		500	ns
T_{VHIGH}	VCLK high-time	4.0		µs
T_{VLOW}	VCLK low-time	4.7		µs
T_{VHZ}	Mode transition time		500	ns
T_{VPU}	Transmit-only power-up time	0		ns

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5V to +5.5V C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.5-volt		Units
		Min	Max	
f_{SCL}	Clock Frequency, SCL	0	100	kHz
t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{HIGH}	Clock Pulse Width High	4.0		µs
t_I	Noise Suppression Time[1] (SDA and SCL pins)		NA	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
$t_{HD.STA}$	Start Hold Time	4.0		µs
$t_{SU.STA}$	Start Set-up Time	4.7		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	250		ns
t_R	Inputs Rise Time[1]		1.0	µs
t_F	Inputs Fall Time[1]		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.0		µs
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		10	ms
Endurance[1]	5.0V, 25°C, Page Mode	1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT24C21 has two modes of operation: the Transmit-only Mode and the Bidirectional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input (SCL and VCLK) and both modes sharing a common Bidirectional data line (SDA). The AT24C21 enters the Transmit-only Mode upon powering up the device. In this mode, the device transmits data on the SDA pin upon a clock signal on the VCLK pin. The device will remain in the Transmit-only Mode until a valid high-to-low transition takes place on the SCL pin. The device will switch into the Bidirectional Mode when a valid transition on the SCL pin is recognized. Once the device has transitioned to the Bidirectional Mode, there is no way to return to the Transmit-only Mode, except to power down (reset) the device.

Transmit-only Mode (DDC1)

The AT24C21 will power up in the Transmit-only Mode. In this mode, the device will output one bit of data on the SDA pin on each rising edge on the VCLK pin. Data is transmitted in 8 bit words with the most significant bit first. Each word is followed by a 9th “don't care” bit which will be in high impedance state (refer to Figure 1). The AT24C21 will continuously cycle through the entire memory array in incremental sequence as long a VCLK is present and no falling edges on SCL are received. When the maximum address (7FH) is reached, the output will wrap around to the zero location (00H) and continue. The Bidirectional mode clock (SCL) pin must be held high for the device to remain in the Transmit-only mode.

Upon power-up, the AT24C21 will not output valid data until it has been initialized. During initialization, data will not be available until after the first nine clocks are sent to the device (refer to Figure 2). The starting address for the Transmit-only mode can be determined during initialization. If the SDA pin is held high during the first eight clocks (refer to Figure 2), the starting address will be 7FH. If the SDA pin is low during the first eight clocks, the starting address will be 00H. During the ninth clock, SDA should be in high impedance.

Figure 1. Transmit-only Mode

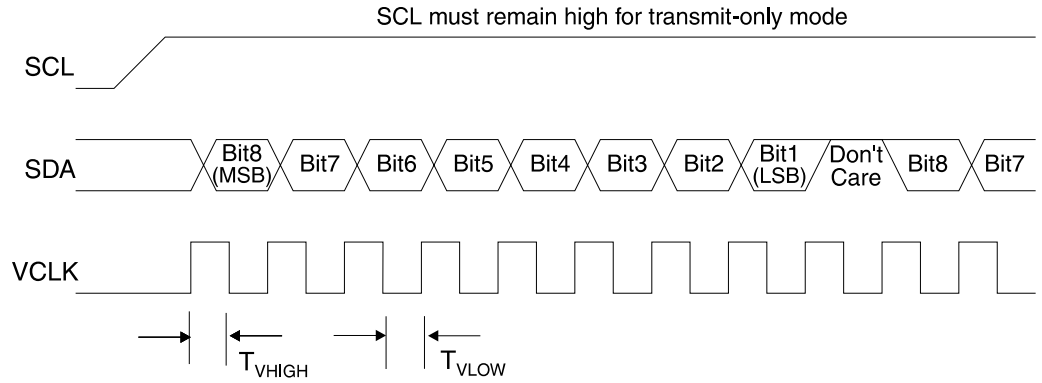
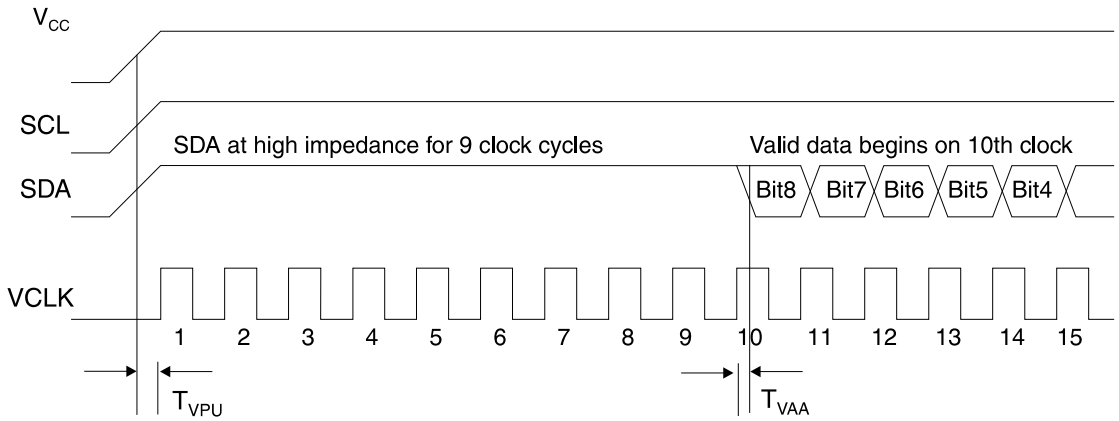


Figure 2. Device Initialization for Transmit-only Mode



Bidirectional Mode (DDC2)

This mode supports a 2-wire, Bidirectional data transmission protocol. The AT24C21 can be switched into the Bidirectional Mode by issuing a valid high to low transition on the SCL pin (refer to Figure 3). After the device is in the Bidirectional Mode, all inputs to the VCLK pin are ignored, except when a logic high is required to enable write capability. All byte and page writes and byte and sequential reads are supported in this mode.

Bidirectional Mode Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read or write sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Device Addressing

The AT24C21 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 4).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next three bits are don't care for the AT24C21.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

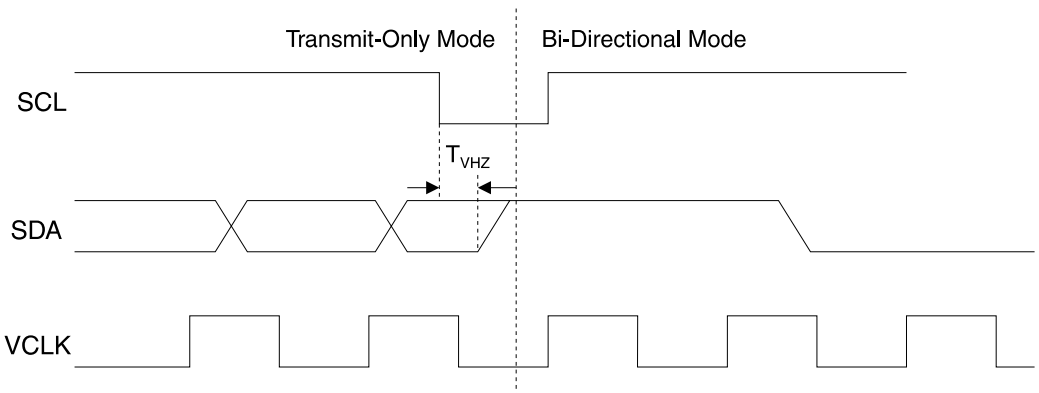
Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

STANDBY MODE: The AT24C21 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

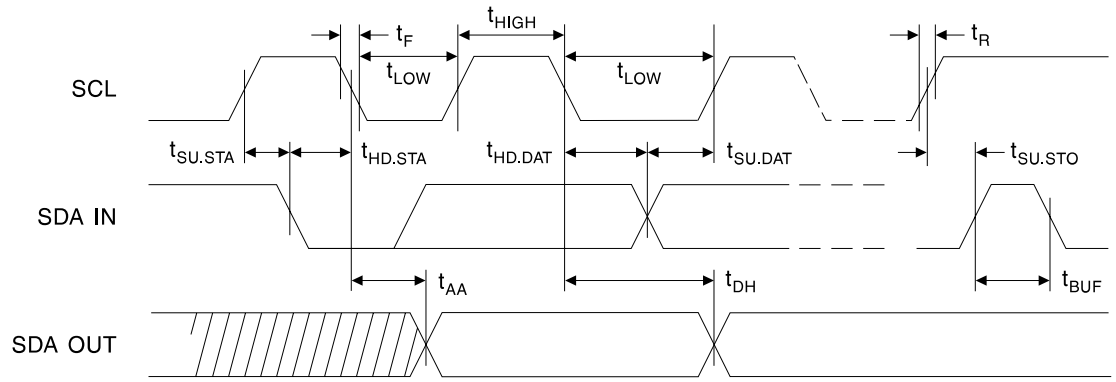
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

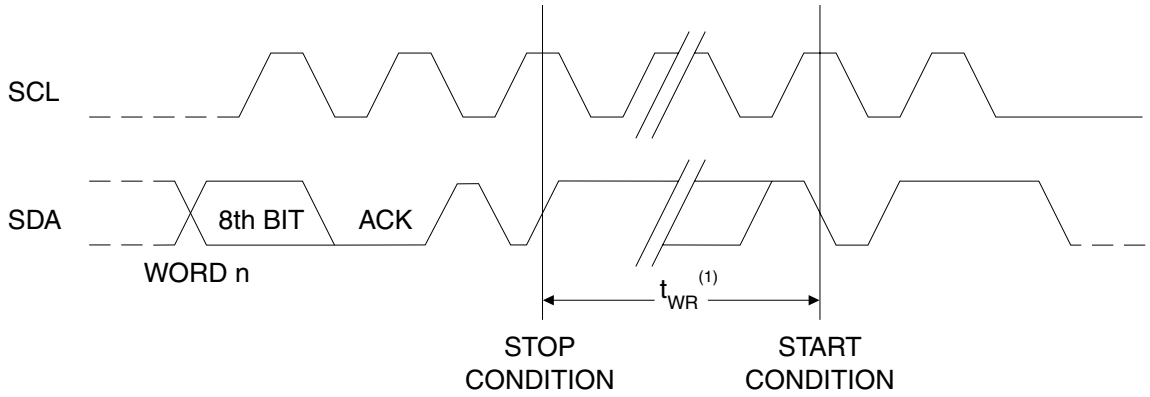
Figure 3. Mode Transition



Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

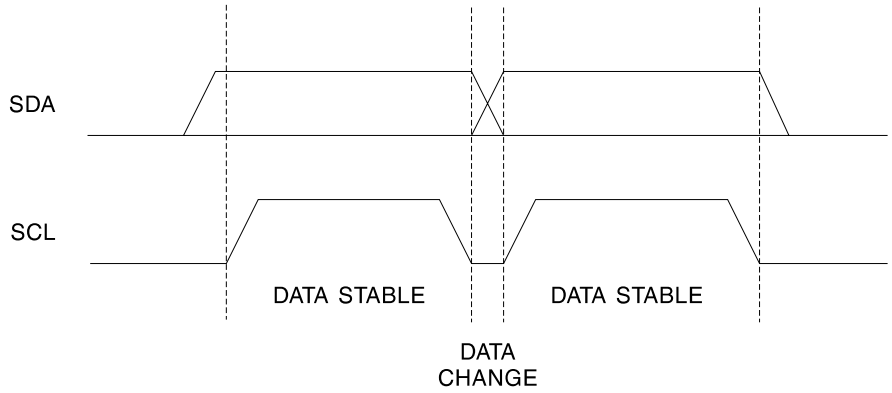


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

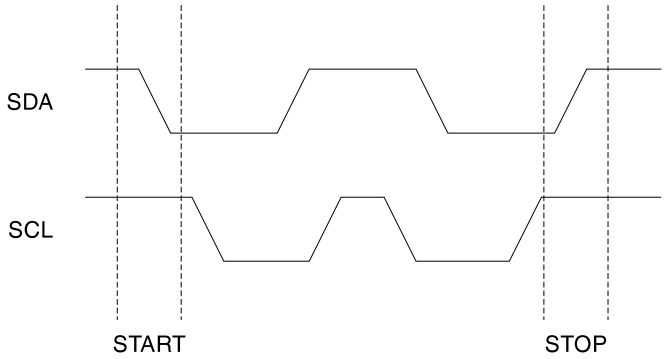


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

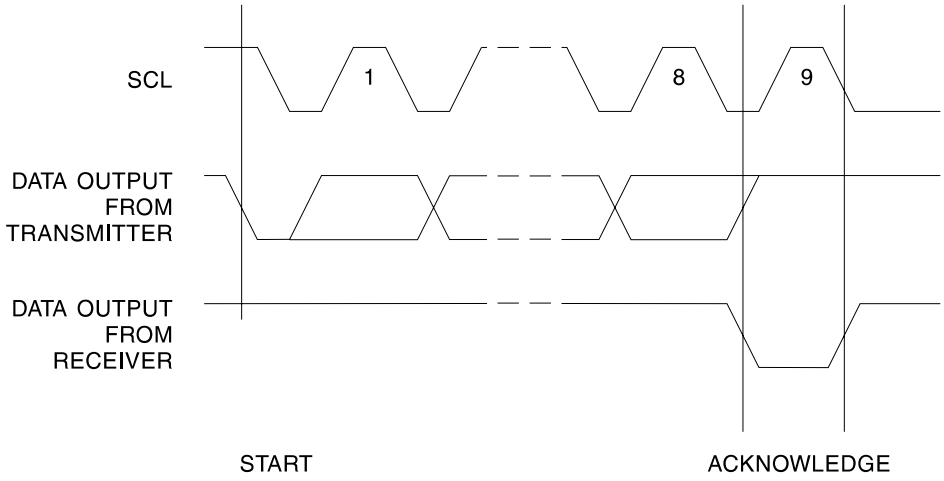
Data Validity



Start and Stop Definition



Output Acknowledge



Write Operations

BYTE WRITE: A write operation requires an 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle , t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 5).

It is required that VCLK be held at a high logic level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

PAGE WRITE: The AT24C21 is capable of an 8-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 6).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

It is required that VCLK be held at a high logic level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

WRITE PROTECTION: When VCLK pin is connected to GND and in the Bidirectional Mode, the entire memory is protected and becomes ROM only. This protects the device memory from any inadvertent write operations.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. Furthermore, the AT24C21 employs a low V_{CC} detector circuit which disables the erase\write logic whenever V_{CC} falls below 1.5 volts.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 7).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 8).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 9).

Figure 4. Device Address

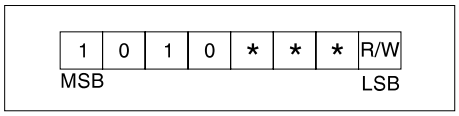


Figure 5. Byte Write

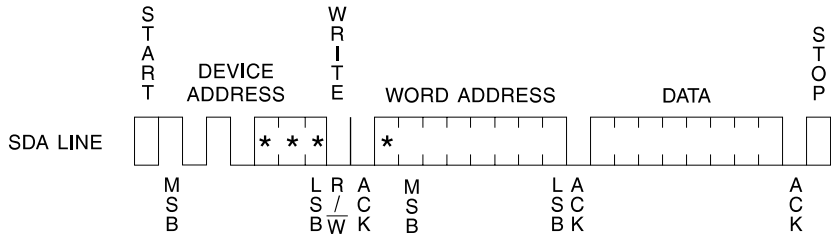
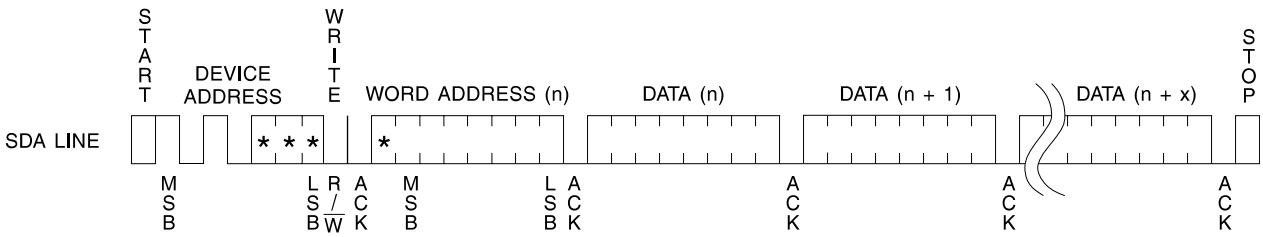


Figure 6. Page Write



(*=Don't care bits)

Figure 7. Current Address Read

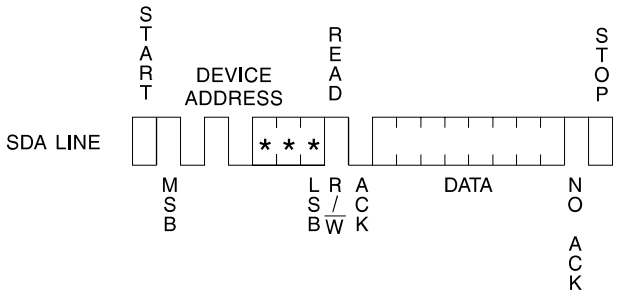


Figure 8. Random Read

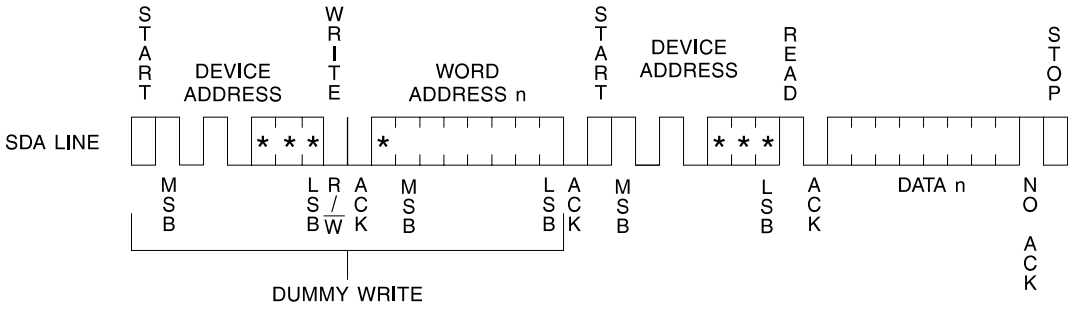
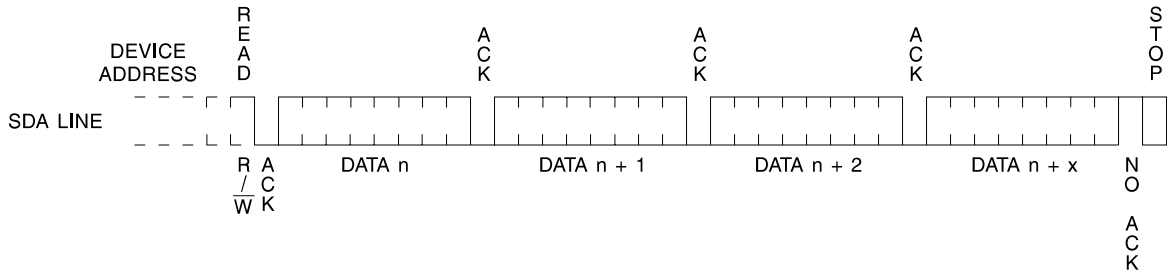


Figure 9. Sequential Read



(*=Don’t care bits)

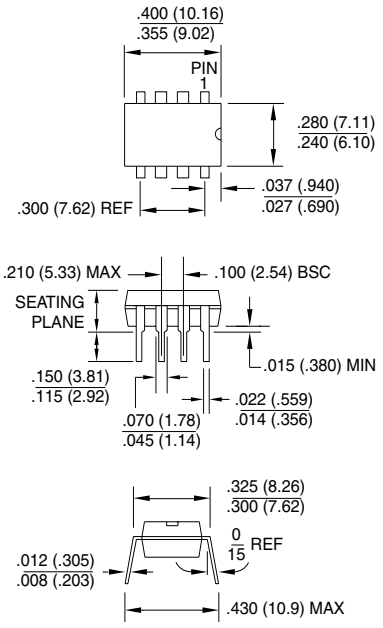
Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	4	100	AT24C21-10PC-2.5 AT24C21-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	3000	4	100	AT24C21-10PI-2.5 AT24C21-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)

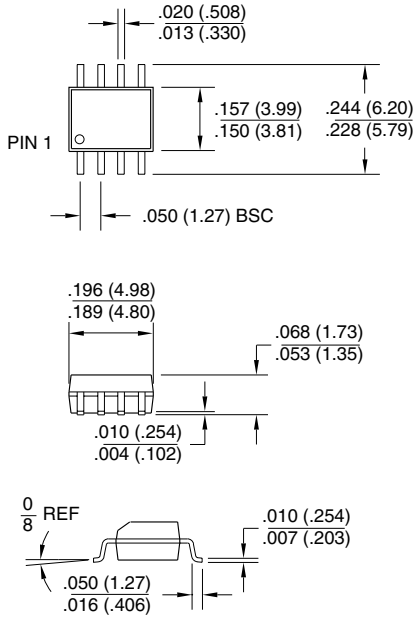
Package Type	
8P3	8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
-2.5	Low Voltage (2.5V to 5.5V)

Packaging Information

8P3, 8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



8S1, 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimension in Inches and (Millimeters)



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