

# NTLLD4901NF

## MOSFET – Power, Dual, N-Channel with Integrated Schottky WDFN, (3 mm x 3 mm)

**30 V, High Side 11 A / Low Side 13 A**

### Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Low Side MOSFET with Integrated Schottky
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

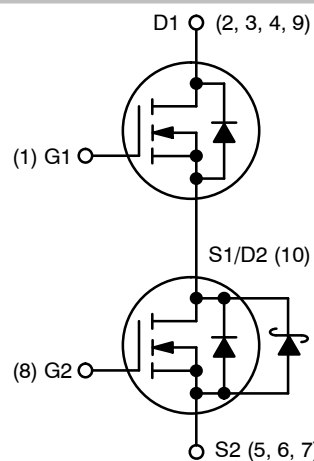
- DC-DC Converters
- System Voltage Rails
- Point of Load



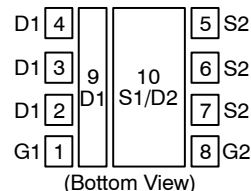
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
Q1 Top FET 30 V	17.4 mΩ @ 10 V	11 A
	25 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	13.3 mΩ @ 10 V	13 A
	20 mΩ @ 4.5 V	



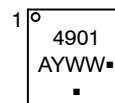
### PIN CONNECTIONS



### MARKING DIAGRAM



WDFN8  
CASE 511BP



- 4901 = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTLLD4901NF

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit		
Drain-to-Source Voltage	Q1	$V_{DSS}$	30	V		
Drain-to-Source Voltage	Q2					
Gate-to-Source Voltage	Q1	$V_{GS}$	$\pm 20$	V		
Gate-to-Source Voltage	Q2					
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	Q1	$I_D$	8.3	A
		$T_A = 85^\circ\text{C}$			6.0	
		$T_A = 25^\circ\text{C}$	Q2		9.6	
		$T_A = 85^\circ\text{C}$			6.9	
Power Dissipation $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	Q1	$P_D$	1.82	W
			Q2		1.88	
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	Q1	$I_D$	11	A
			Q2		8	
		$T_A = 25^\circ\text{C}$	Q2		13	
		$T_A = 85^\circ\text{C}$			9.1	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	Q1	$P_D$	3.23	W
			Q2		3.27	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	Q1	$I_D$	5.5	A
			Q2		4.0	
		$T_A = 25^\circ\text{C}$	Q2		6.3	
		$T_A = 85^\circ\text{C}$			4.5	
Power Dissipation $R_{\theta JA}$ (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	Q1	$P_D$	0.80	W
			Q2		0.81	
Pulsed Drain Current	Steady State	$T_A = 25^\circ\text{C}$ $t_p = 10 \mu\text{s}$	Q1	$I_{DM}$	65	A
			Q2		70	
Operating Junction and Storage Temperature			Q1	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
			Q2			
Source Current (Body Diode)			Q1	$I_S$	4.2	A
			Q2		6.0	
Drain to Source DV/DT				$dV/dt$	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 9.0$ A <sub>pk</sub> , $L = 0.3$ mH, $R_G = 25 \Omega$ )			Q1	EAS	12	mJ
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 9.5$ A <sub>pk</sub> , $L = 0.3$ mH, $R_G = 25 \Omega$ )			Q2	EAS	13.5	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)				$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu
- Surface-mounted on FR4 board using the minimum recommended pad size of 90 mm<sup>2</sup>

# NTLLD4901NF

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	FET	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	Q1	R <sub>θJA</sub>	68.8	°C/W
	Q2		66.4	
Junction-to-Ambient – Steady State (Note 4)	Q1	R <sub>θJA</sub>	156.4	
	Q2		153.9	
Junction-to-Ambient – (t ≤ 10 s) (Note 3)	Q1	R <sub>θJA</sub>	38.7	
	Q2		38.2	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu

4. Surface-mounted on FR4 board using the minimum recommended pad size of 90 mm<sup>2</sup>

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>							
Drain-to-Source Break-down Voltage	Q1	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
	Q2			30			
Drain-to-Source Break-down Voltage Temperature Coefficient	Q1	V <sub>(BR)DSS</sub> / T <sub>J</sub>			18		mV / °C
	Q2				15		
Zero Gate Voltage Drain Current	Q1	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		1	μA
				T <sub>J</sub> = 125°C		10	
	Q2		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		500	
Gate-to-Source Leakage Current	Q1	I <sub>GSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = ±20 V			±100	nA
	Q2					±100	

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	Q1	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.2		2.2	V	
	Q2			1.2		2.2		
Negative Threshold Temperature Coefficient	Q1	V <sub>GS(TH)</sub> / T <sub>J</sub>			4.5		mV / °C	
	Q2				4.0			
Drain-to-Source On Resistance	Q1	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 9 A		14	17.4	mΩ
			V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 9 A		20	25	
	Q2		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A		11	13.3	
			V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 11 A		16	20	
Forward Transconductance	Q1	g <sub>FS</sub>	V <sub>DS</sub> = 1.5 V, I <sub>D</sub> = 9 A		16		S	
	Q2				18			

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	Q1	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 15 V		605		pF
	Q2				660		
Output Capacitance	Q1	C <sub>OSS</sub>			190		
	Q2				325		
Reverse Capacitance	Q1	C <sub>RSS</sub>			102		
	Q2				17.5		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

6. Switching characteristics are independent of operating junction temperatures.

# NTLLD4901NF

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	-----	--------	----------------	-----	-----	-----	------

### CHARGES, CAPACITANCES & GATE RESISTANCE

Total Gate Charge	Q1	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 9 A		6.5		nC	
	Q2				5.0			
Threshold Gate Charge	Q1	Q <sub>G(TH)</sub>			1.1			
	Q2				1.1			
Gate-to-Source Charge	Q1	Q <sub>GS</sub>			1.9			
	Q2				2.0			
Gate-to-Drain Charge	Q1	Q <sub>GD</sub>			3.2			
	Q2				1.46			
Total Gate Charge	Q1	Q <sub>G(TOT)</sub>		V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 9 A		12		nC
	Q2					10.6		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9 A, R <sub>G</sub> = 3.0 Ω		8.0		ns
	Q2				7.5		
Rise Time	Q1	t <sub>r</sub>			7.2		
	Q2				11.2		
Turn-Off Delay Time	Q1	t <sub>d(OFF)</sub>			11		
	Q2				11.6		
Fall Time	Q1	t <sub>f</sub>			3.3		
	Q2				1.9		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9 A, R <sub>G</sub> = 3.0 Ω		4.2		ns
	Q2				4.3		
Rise Time	Q1	t <sub>r</sub>			11.6		
	Q2				11.4		
Turn-Off Delay Time	Q1	t <sub>d(OFF)</sub>			14.1		
	Q2				14.3		
Fall Time	Q1	t <sub>f</sub>			2.0		
	Q2				1.3		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Voltage	Q1	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A	T <sub>J</sub> = 25°C	0.80	1.2	V
				T <sub>J</sub> = 125°C	0.65		
	Q2		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A	T <sub>J</sub> = 25°C	0.50	0.80	
				T <sub>J</sub> = 125°C	0.45		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

6. Switching characteristics are independent of operating junction temperatures.

# NTLLD4901NF

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
Reverse Recovery Time	Q1	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, d <sub>IS</sub> /d <sub>t</sub> = 100 A/μs, I <sub>S</sub> = 3 A		17.9		ns
	Q2				23.3		
Charge Time	Q1	t <sub>a</sub>			9.0		
	Q2				11.3		
Discharge Time	Q1	t <sub>b</sub>			9.0		
	Q2				12		
Reverse Recovery Charge	Q1	Q <sub>RR</sub>			8.0		nC
	Q2				12		

## PACKAGE PARASITIC VALUES

Source Inductance	Q1	L <sub>S</sub>	T <sub>A</sub> = 25°C		0.36		nH
	Q2				0.36		
Drain Inductance	Q1	L <sub>D</sub>			0.054		nH
	Q2				0.054		
Gate Inductance	Q1	L <sub>G</sub>			1.3		nH
	Q2				1.3		
Gate Resistance	Q1	R <sub>G</sub>			0.8		Ω
	Q2				0.8		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

6. Switching characteristics are independent of operating junction temperatures.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTLLD4901NFTWG	WDFN8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS – Q1

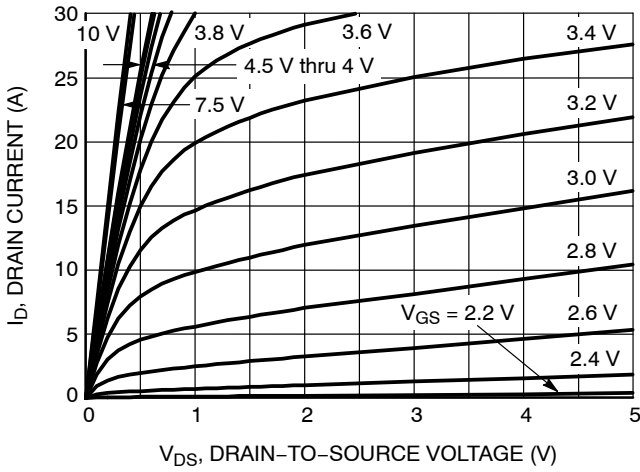


Figure 1. On-Region Characteristics

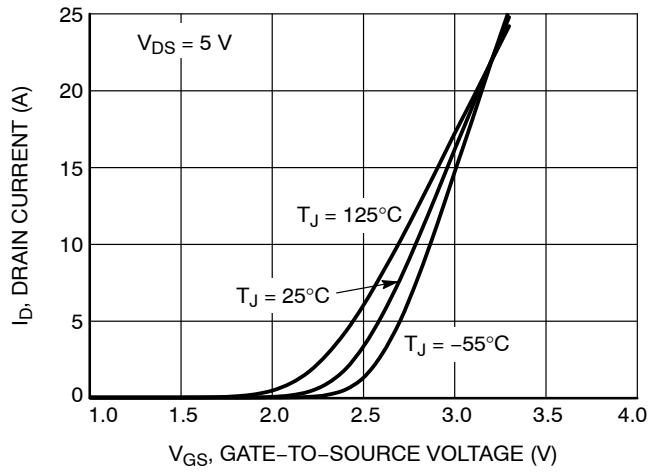


Figure 2. Transfer Characteristics

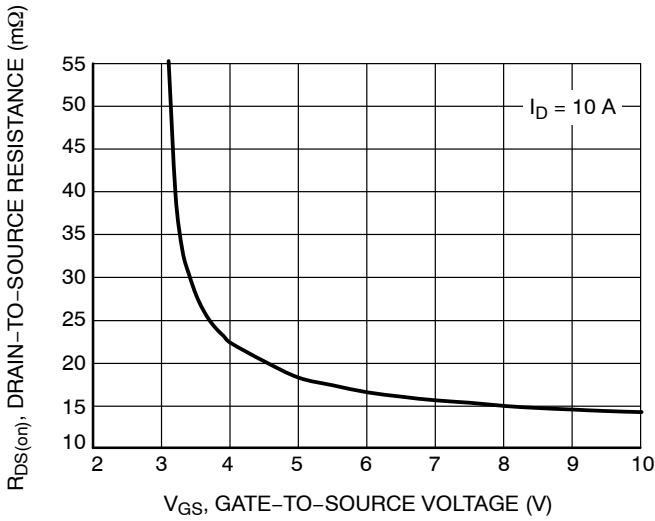


Figure 3. On-Resistance vs. Gate-to-Source Resistance

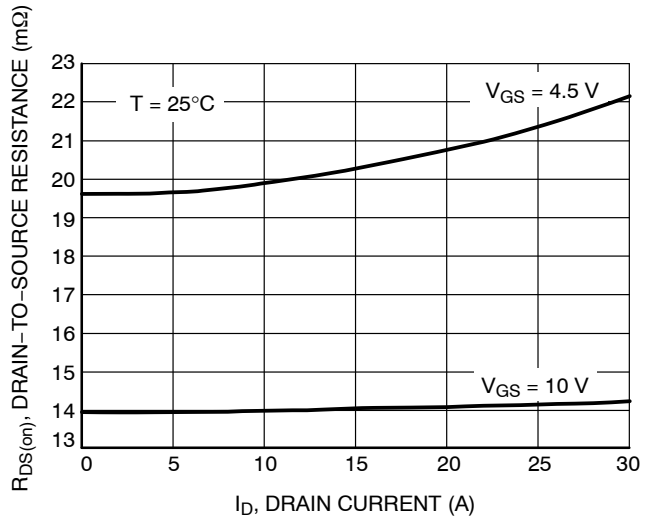


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

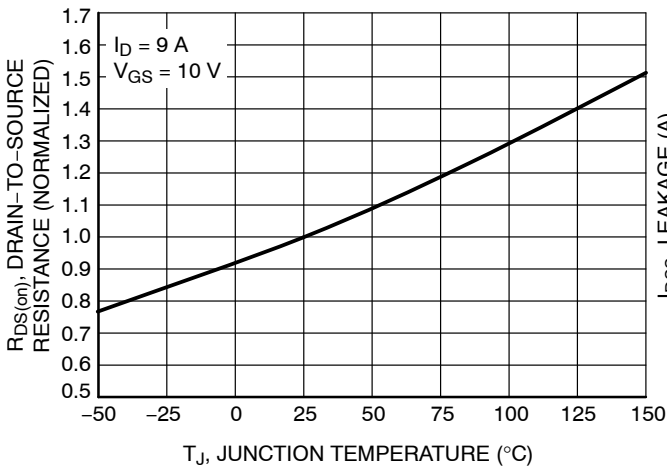


Figure 5. On-Resistance Variation with Temperature

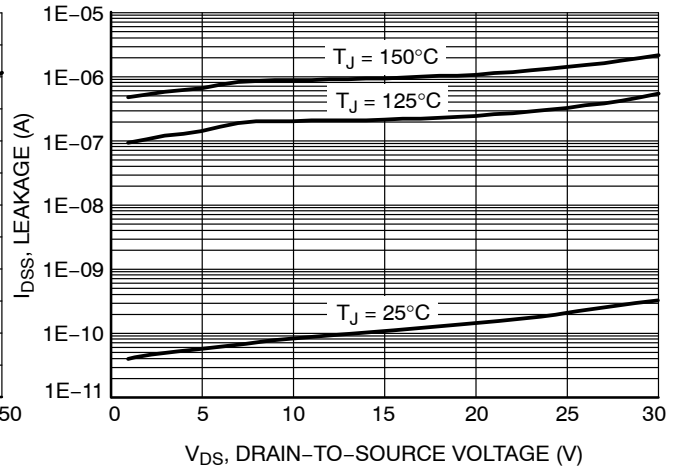
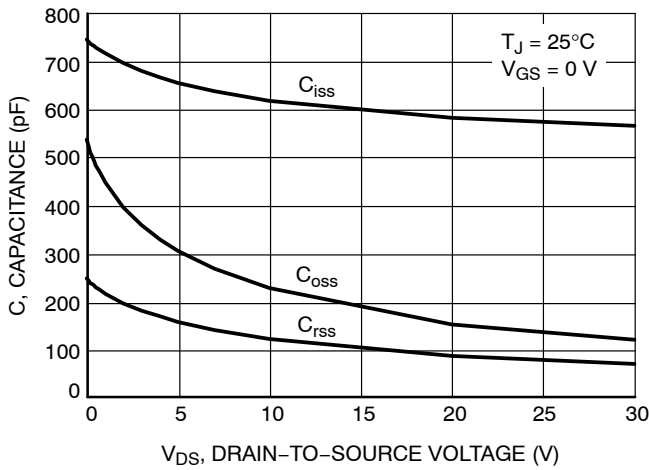


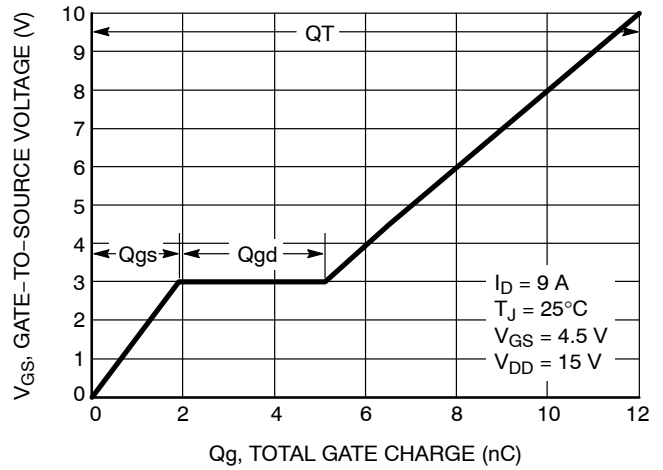
Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTLLD4901NF

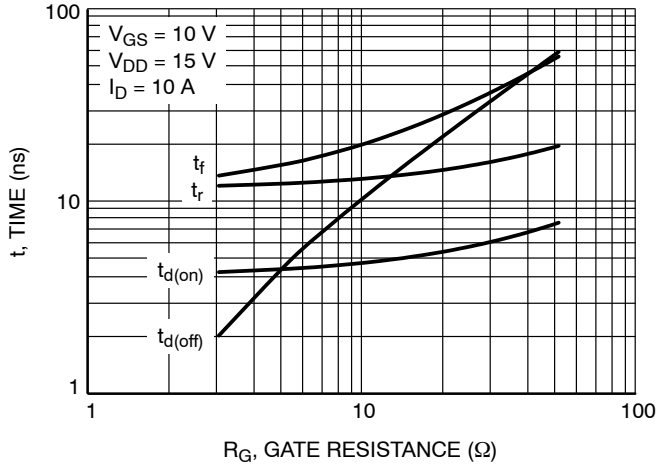
## TYPICAL CHARACTERISTICS – Q1



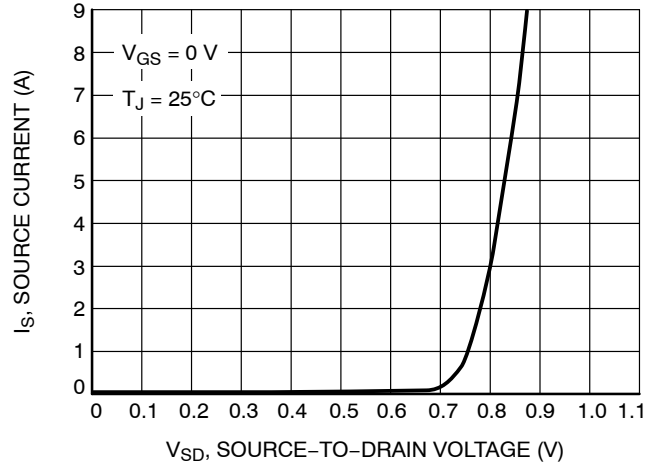
**Figure 7. Capacitance Variation**



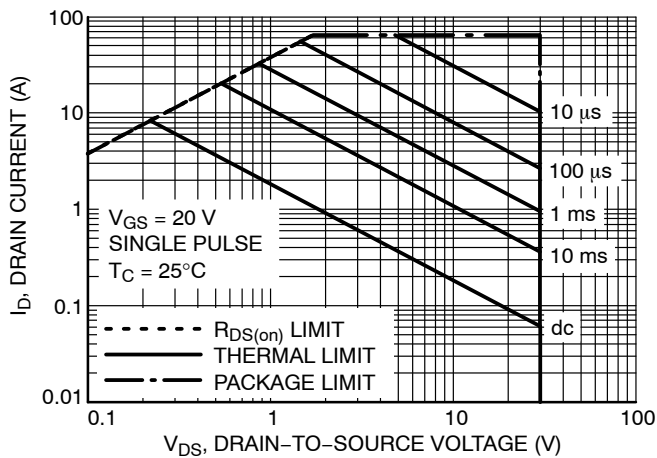
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



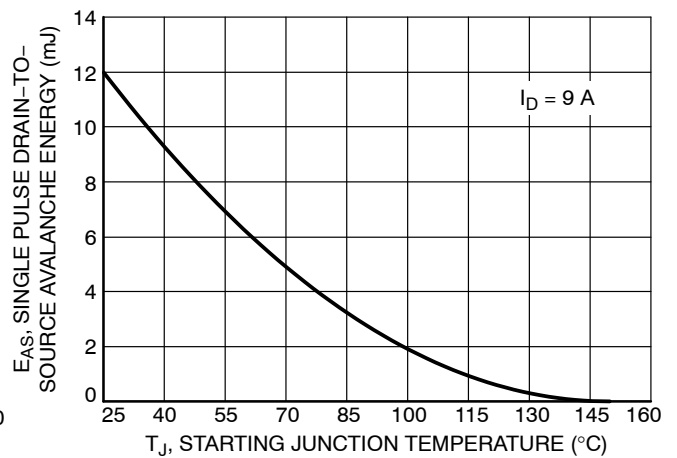
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

# NTLLD4901NF

## TYPICAL CHARACTERISTICS – Q1

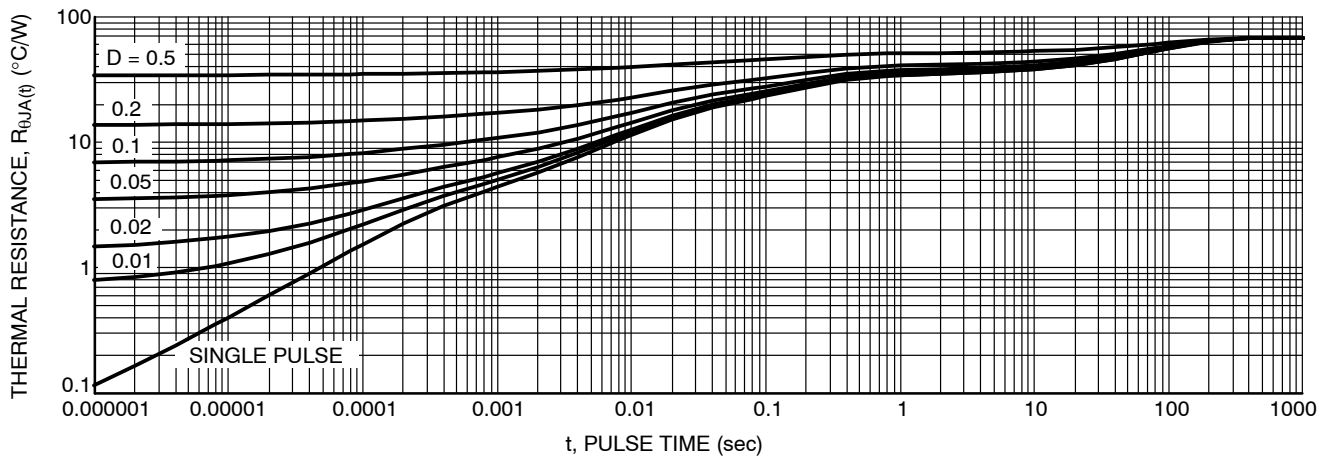


Figure 13. Thermal Response



TYPICAL CHARACTERISTICS – Q2

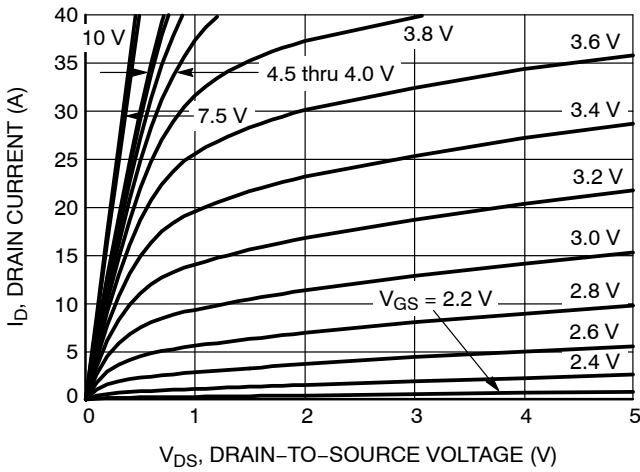


Figure 14. On-Region Characteristics

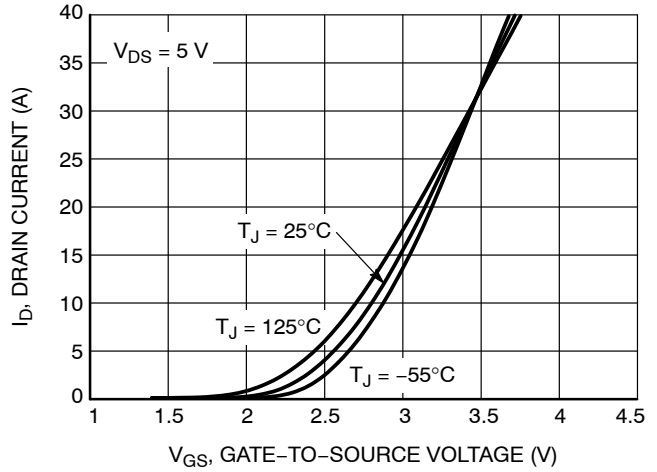


Figure 15. Transfer Characteristics

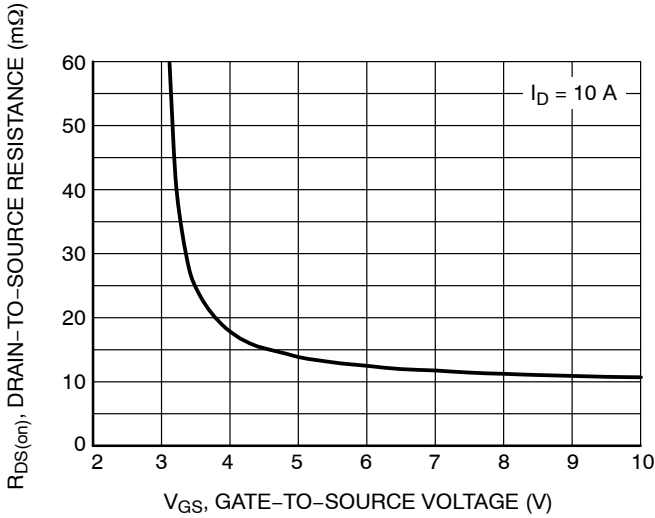


Figure 16. On-Resistance vs. Gate-to-Source Resistance

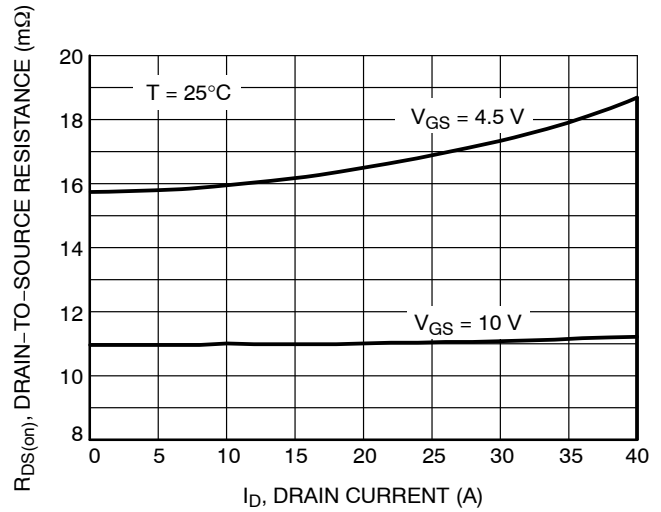


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

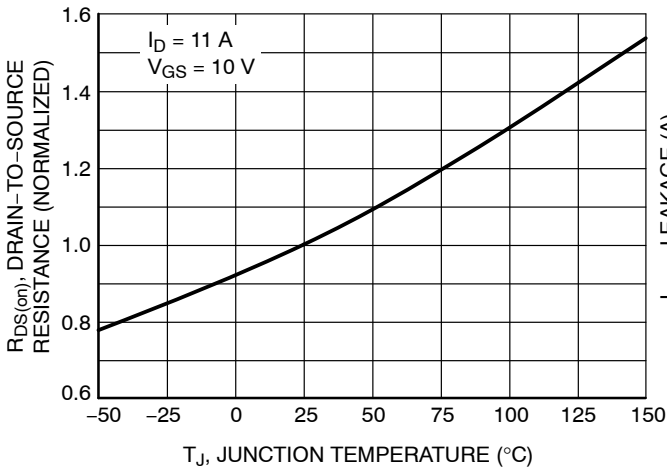


Figure 18. On-Resistance Variation with Temperature

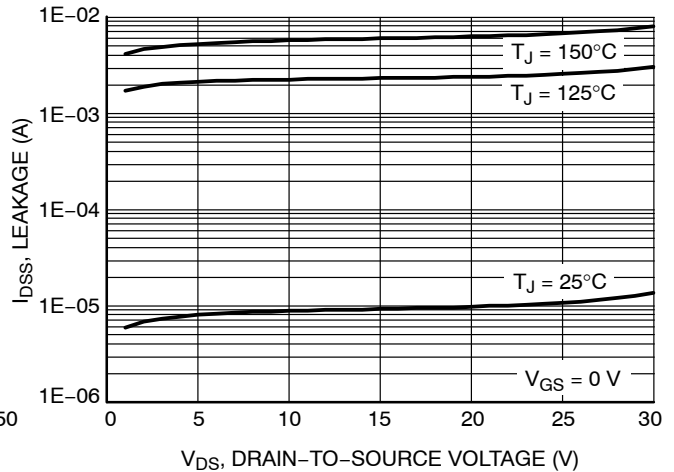
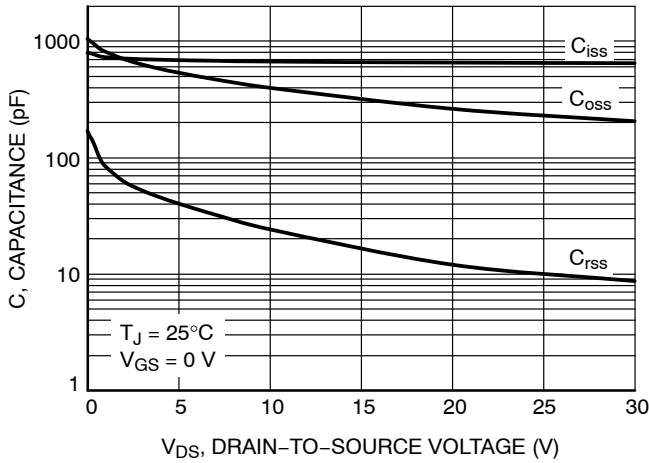


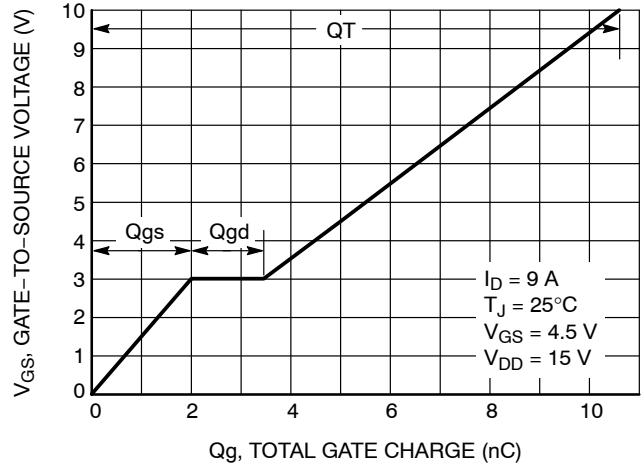
Figure 19. Drain-to-Source Leakage Current vs. Voltage

# NTLLD4901NF

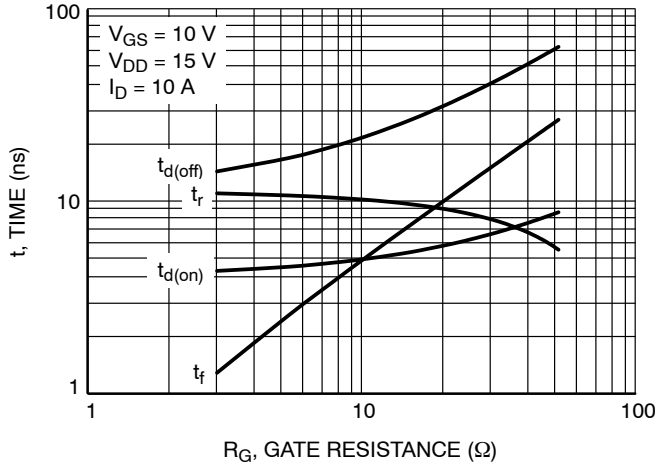
## TYPICAL CHARACTERISTICS – Q2



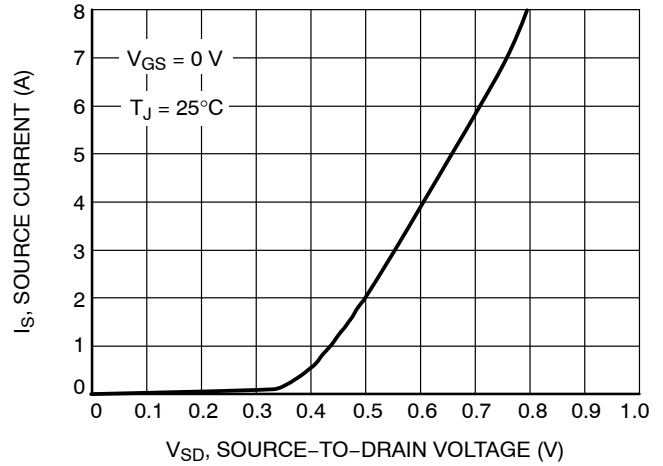
**Figure 20. Capacitance Variation**



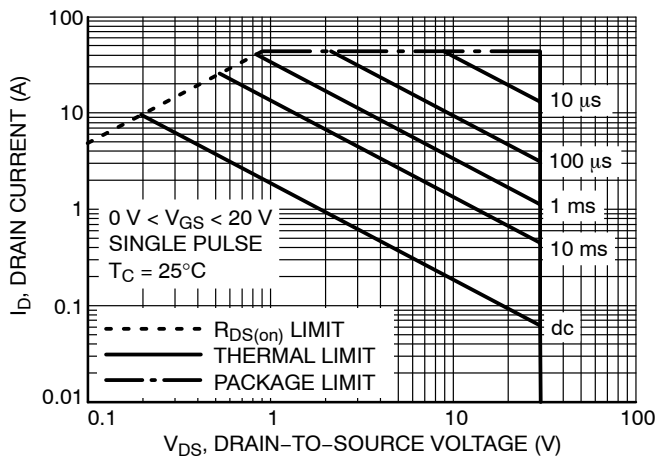
**Figure 21. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



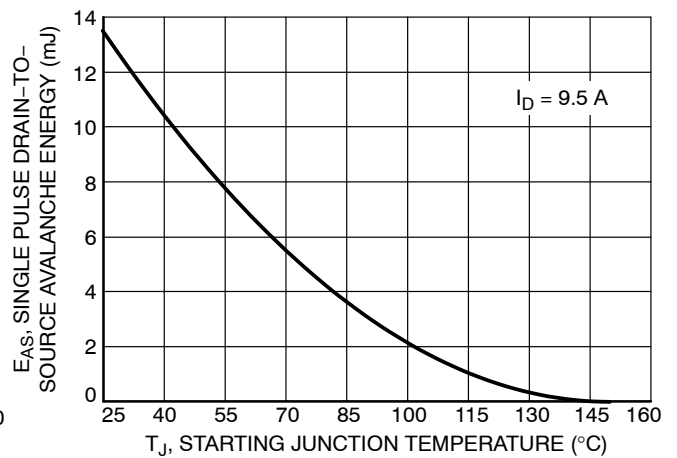
**Figure 22. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 23. Diode Forward Voltage vs. Current**



**Figure 24. Maximum Rated Forward Biased Safe Operating Area**



**Figure 25. Maximum Avalanche Energy vs. Starting Junction Temperature**

# NTLLD4901NF

## TYPICAL CHARACTERISTICS – Q2

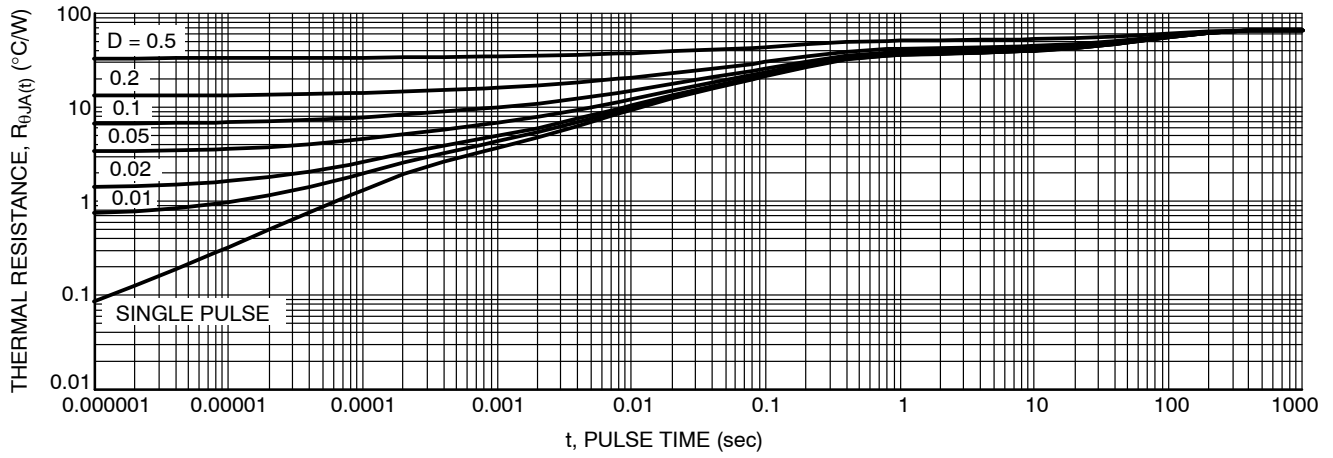


Figure 26. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

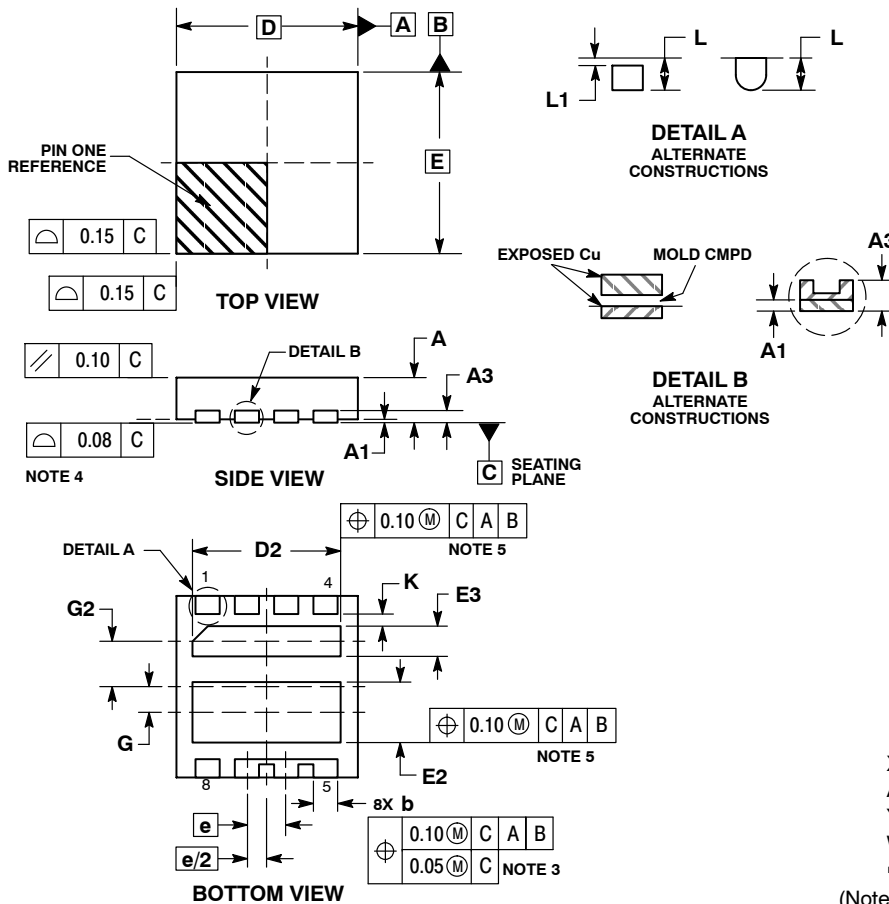
ON Semiconductor®



SCALE 2:1

WDFN8 3x3, 0.65P  
CASE 511BP  
ISSUE B

DATE 17 JUL 2012

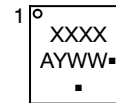


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.05 AND 0.15 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE EXPOSED PADS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.30	0.50
D	3.00 BSC	
D2	2.35	2.55
E	3.00 BSC	
E2	0.90	1.10
E3	0.40	0.60
e	0.65 BSC	
G	0.43 BSC	
G2	0.68 BSC	
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

**GENERIC MARKING DIAGRAM\***

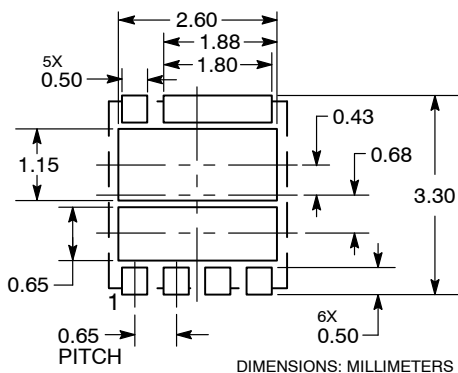


- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**RECOMMENDED SOLDERING FOOTPRINT\***



- STYLE 1:**
1. GATE 1
  2. DRAIN 1
  3. DRAIN 1
  4. DRAIN 1
  5. SOURCE 2
  6. SOURCE 2
  7. SOURCE 2
  8. GATE 2
  9. DRAIN 1
  10. SOURCE 1/DRAIN 2

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON53342E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN8, 3X3, 0.65P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)