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APPLICATION NOTE 5273

Understanding and Configuring the DS2483 1-Wire® Master

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Abstract: The DS2483 represents the next generation of integrated 1-Wire masters. With its configurability, 2-stage power-savings mode, and level translator function, the DS2483 is well suited for battery-operated applications. This application note explains the operation of the 1-Wire master port, gives advice on when to deviate from the default configurations, and explains how to determine the drive capability for a given network.

Introduction

The DS2483 is the latest member of the family of integrated 1-Wire masters (**Table 1**). The device builds upon the DS2482 1-Wire masters by adding configurability and a level shifter, enabling the I²C and 1-Wire port to operate on different voltages. Battery-operated equipment will benefit from the 2-stage power-savings mode, where the master function and the 1-Wire bus can be shut down independently. With just one additional command and register, existing firmware for the DS2482, as described in application note 3684, "How to Use the DS2482 I²C 1-Wire Master," can easily be adapted to take advantage of the DS2483's improvements. This application note explains the major features, gives guidance on how to use them, and provides instructions on how to determine whether the DS2483 can drive a given 1-Wire network at standard or overdrive speed. Table 1 compares the features of the DS2483 to other Maxim 1-Wire masters.

Table 1. A Comparison of the DS2483 to Other 1-Wire Masters*

Feature	DS2483	DS2482	DS2480B
Host Port Type	I²C	I²C	RXTX
Host Port Voltage	1.8V, 3.3V, 5.0V	3.3V, 5.0V	5.0V
Low-Power Mode	Yes	DS2482-101 only	No
1-Wire Pullup Voltage	1.7V to 5.25V	3.3V, 5.0V	5.0V
1-Wire Pullup Type	Resistive, switched	Resistive, switched	Current source, switched
Slew Rate Control	Falling edge, fast	Rising and falling edge, slow	Falling edge, 0.55V/µs to 15V/µs (STD), 15V/µs (OD)
1-Wire Input High Voltage	0.6 × V_{CC} (min)	1.9V (min) (V_{CC} = 3.3V), 3.4V (V_{CC} = 5.0V)	3.4V (min)
1-Wire Input Low Voltage	0.2 × V_{CC} (max)	0.9V (max) (V_{CC} = 3.3V), 1.2V (V_{CC} = 5.0V)	1.8V (max)
Reset/Presence Detect Cycle	880µs to 1480µs (STD), 88µs to 148µs (OD)	1184µs (STD), 146µs (OD)	1096µs (STD), 138µs (OD)
Presence Pulse Detect	58µs to 76µs (STD), 5.5µs to 11µs (OD)	70µs (STD), 7.5µs (OD)	72µs (STD), 10µs (OD)
t_{W1L} Duration	8µs (STD), 0.75µs (OD)	8µs (STD), 1.0µs (OD)	8µs to 15µs (STD), 1.0µs (OD)
Read Sample Time	12µs (STD), 1.75µs (OD)	14µs (STD), 1.5µs (OD)	11µs to 25µs (STD), 2µs (OD)
t_{REC0} Duration	2.75µs to 25.25µs (STD and OD)	5.3µs (STD), 3.0µs (OD)	3µs to 10µs (STD), 3µs (OD)
t_{W0L} Duration	52µs to 70µs (STD), 5µs to 10µs (OD)	64µs (STD), 7.5µs (OD)	57µs (STD), 7µs (OD)
Time Slot Duration	t_{W0L} + t_{REC0}	69.3µs (STD), 10.5µs (OD)	t_{W1L} + t_{REC0} + 49µs (STD, write-1, read), t_{W0L} + t_{REC0} (STD, write-0), 10µs (OD)
Active Pullup Threshold	1.2V (max)	Approx. V_{CC}/2	1.2V (max)
Active Pullup Duration	t_{REC0} (min), t_{SLOT} - t_{W1L} (max)	2.5µs (STD), 0.5µs (OD)	Load dependent, automatic

*All underlined text in table indicates configurability.

DS2483 Configurability

The DS2483 has a total of nine configurable parameters. Five of these are of binary type, i.e., they are either on or off. The other four parameters could have up to 16 different values. For backwards compatibility to the DS2482 series of 1-Wire masters, four of the binary parameters are configured through the Device Configuration register. These parameters are **active pullup**, **strong pullup**, **1-Wire speed**, and the new function **1-Wire Power Down**. The fifth binary parameter, **weak pullup resistor** value, and the timing parameters **reset low time**, **presence pulse sampling time**, **write-zero low time**, and **write-zero recovery time**, are configured through the Port Configuration register.

Device Configuration Register

Except for the definition of one bit, this register functions the same way with the DS2483 as it does with the DS2482. Write access is established through the Write Device Configuration command. The setting can be verified through a subsequent I²C read access. For random read access, first use the Set Read Pointer command with the pointer code of the Device Configuration register and then perform an I²C read access to the device. Unless the default settings are acceptable for the application, the device configuration needs to be updated after a power-on reset (POR) and after a Device Reset command.

Device Configuration Register Bit Descriptions

APU Active Pullup

Function: Enables extra power delivery during 1-Wire communication. The power delivery ends with the time slot, is active only for a very short time (0.5µs or 2.5µs) during a presence-detect cycle. If APU is not set, weak pullup applies, which heavily limits the number of 1-Wire slaves that the network can handle. See section *How the DS2483 Performs 1-Wire Communication* for more information.

Usage: Normally APU should be set. It must be set when using overdrive speed (OD). The only case where APU should not be set is when using the add-on circuit in Figure 7 of application note 4931, "IEEE 1451.4 Class 1 MMI Smart Transducer Digital Driver Circuit."

Note: Once set, APU remains set until the DS2483 performs a POR, receives a Device Reset command, or the bit is written to 0.

SPU Strong Pullup

Function: Enables extra power delivery that starts on the rising edge of the 8th time slot generated through the 1-Wire Write Byte command or on the rising edge of a time slot generated through the 1-Wire Single Bit command. The power delivery continues *beyond the time slot* and typically ends when the DS2483 receives another command that generates 1-Wire activity, or when the SPU bit is written to 0.

Usage: Strong pullup is used with 1-Wire slaves that at certain times need power for an extended time, such as when writing to EEPROM, or performing a SHA computation or a temperature conversion without having V_{CC} power.

Note: SPU automatically returns to 0 with subsequent 1-Wire activity (1-Wire reset, time slots), when a

POR occurs, or when executing a Device Reset command. Changing the logic level at the SLPZ pin from 1 to 0 and back to 1 does not reset SPU. In other words, if the power delivery is already on, then it continues during and after sleep mode. Therefore, it is recommended to reset the SPU bit *before* activating the sleep mode. The SPU bit must be written to 0 when activating the 1-Wire power-down mode (see the PDN bit description).

1WS 1-Wire Speed

Function: Changes the 1-Wire speed from standard (0, power-on default) to overdrive (1) and vice versa.

Usage: All 1-Wire slaves run on standard speed and most slaves also support overdrive speed, which is approximately 8 times faster. Overdrive speed works only if the network is small enough to ensure a proper recharge as needed for reading a logic 1 during the write-one/read-one time slot. For more details see the *How the DS2483 Performs 1-Wire Communication* section. As part of the power-up procedure, the host could issue the Overdrive Skip ROM command at standard speed, change the 1WS and APU bit to 1, and then issue a 1-Wire Reset command, after which all 1-Wire communication takes place at overdrive speed.

Note: Once set, 1WS remains set until the DS2483 performs a POR, receives a Device Reset command, or the bit is written to 0.

PDN 1-Wire Power-Down

Function: Removes power from the 1-Wire bus (weak pullup, active pullup).

Usage: Battery-operated equipment often includes 1-Wire devices that do not need to be powered all the time. The 1-Wire power-down feature helps conserving battery energy by shutting down the 1-Wire bus. As a consequence, the 1-Wire slaves lose any volatile data (e.g., their status). Up to 300µA are saved if the host in the next step changes the logic level at the SLPZ pin from 1 to 0, which shuts down the DS2483. If the application requires for the 1-Wire slaves to maintain their status, keep PDN at 0 and change the logic level at SLPZ to 0.

Note: When writing to the device configuration register with PDN = 1 to activate the 1-Wire power-down mode, make sure that the SPU bit is 0. Once set, PDN remains set until the DS2483 performs a POR, receives a Device Reset command, or the bit is written to 0. If PDN is set, 1-Wire communication is not possible.

Port Configuration Register

This register is new with the DS2483. Write access is established through the Adjust 1-Wire Port command. The setting can be verified sequentially through a subsequent I²C read access. For random read access, first use the Set Read Pointer command with the pointer code of the Port Configuration register and then perform an I²C read access to the device. The power-on default settings are chosen to work with the majority of 1-Wire slaves in a 5V environment. A typical reason for changing the settings is a low-voltage environment where some 1-Wire slaves have special timing requirements. Unless the default settings are acceptable for the application, the port configuration needs to be updated after a POR and a Device Reset command.

Port Configuration Register Parameter Descriptions

Reset Low Time (t_{RSTL}, Parameter 000)

Function: Determines the duration of the reset/presence-detect cycle, which is twice the duration of t_{RSTL} (see **Figure 5**). The settings for standard and overdrive speed are independent of each other.

Range: 440µs to 740µs (standard speed), 44µs to 74µs (overdrive speed).

Usage: To accommodate 1-Wire slaves with unusual timing requirements at the system's V_{CC} level (= 1-Wire pullup voltage).

Note: none

Presence Pulse Sampling Time (t_{MSP}, Parameter 001)

Function: Determines the instant t_{MSP} when the 1-Wire bus is sampled to detect a presence pulse (Figure 5). The settings for standard and overdrive speed are independent of each other.

Range: 58µs to 76µs (standard speed), 5.5µs to 11µs (overdrive speed).

Usage: To accommodate 1-Wire slaves with unusual timing requirements at the system's V_{CC} level (= 1-Wire pullup voltage).

Note: none

Write-Zero Low Time (t_{W0L}, Parameter 010)

Function: Determines the duration of the write-zero low time, t_{W0L} (Figure 2). The settings for standard and overdrive speed are independent of each other.

Range: 52µs to 70µs (standard speed), 5.0µs to 10µs (overdrive speed).

Usage: To accommodate 1-Wire slaves with unusual timing requirements at the system's V_{CC} level (= 1-Wire pullup voltage).

Note: The write-zero low time affects the time slot duration (1-Wire data rate).

Write-Zero Recovery Time (t_{REC0}, Parameter 011)

Function: Determines the duration of the write-zero recovery time, t_{REC0} (Figure 2). The setting applies to both standard and overdrive speed.

Range: 2.75µs to 25.25µs

Usage: To improve the power-delivery performance, in particular for large networks, and to accommodate 1-Wire slaves with unusual timing requirements at a very low V_{CC} level (= 1-Wire pullup voltage).

Note: The write-zero recovery time affects the time slot duration (1-Wire data rate).

Weak Pullup Resistor (R_{WPU}, Parameter 100)

Function: Determines the value of the weak 1-Wire pullup resistor, R_{WPU} (R2, R3 in Figure 1). The setting applies to both standard and overdrive speed.

Range: 500Ω to 1000Ω

Usage: To accommodate slaves in a very low V_{CC} environment.

Note: Before choosing the 500Ω value, verify that the resulting low voltage meets the V_{IL} requirements of the DS2483 and all 1-Wire slaves on the bus.

1-Wire Master Port Circuit

To take full advantage of the DS2483, it is important to understand the operation of its 1-Wire master port. Figure 1 shows a model with the main components that affect its operation. Q1 generates reset pulses, write time slots, and starts read time slots. If the APU bit in the Device Configuration register is set, Q2 provides the active pullup when Q1 has stopped pulling the 1-Wire bus low. Q2 also controls the power delivery function, which can be temporarily enabled through the SPU bit (Device Configuration register). Q3 and Q4 select between the two weak 1-Wire pullup resistor options. Typically, Q3 is conducting, which activates the 1000Ω resistor. If the DS2483 is configured for 500Ω, Q3 is off, and Q4 is on. Both Q3 and Q4 are off when Q1 is on. They are also off while the 1-Wire bus is powered down (PDN = 1); under this condition, Q1 is on to ensure a rapid discharge. The voltage on the 1-Wire bus is monitored by two comparators U1 and U2. U1 compares against the threshold V_{IAPO}, which determines when Q2 can turn on to accelerate the bus recharge. U2 compares against the V_{IH1} threshold, determining whether a read time slot conveys a 1 or 0, or whether a presence pulse is detected during a reset/presence-detect cycle. The transistors are controlled by the 1-Wire port configuration and control unit, which receives its input from the comparators U1, U2, and the I²C host.

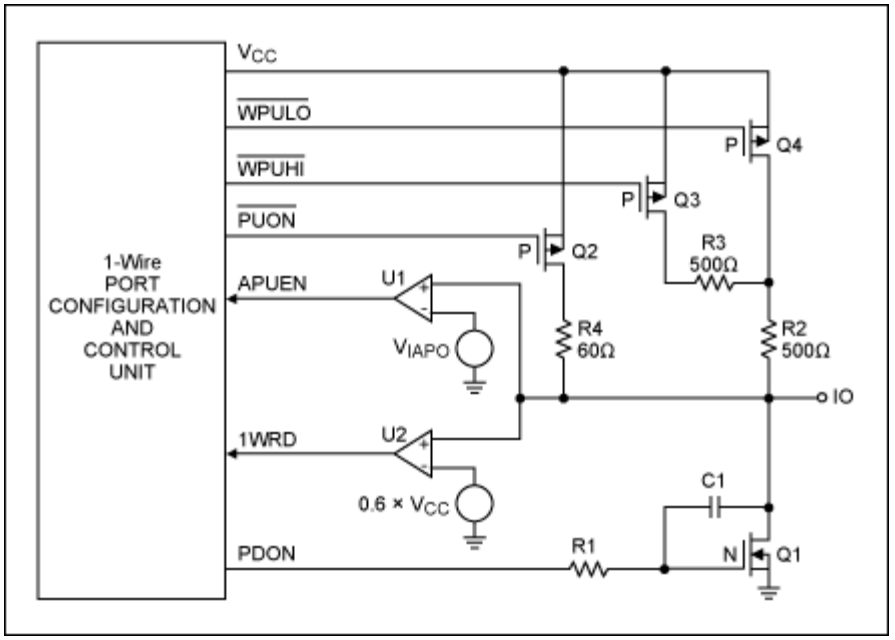

Figure 1. Functional equivalent of the DS2483 1-Wire master port.

How the DS2483 Performs 1-Wire Communication

Watching 1-Wire communication reveals four distinct signal types, called write-zero time slot, write-one/read-one time slot, read-zero time slot, and reset/presence-detect cycle. Communication can take place at two speeds, standard speed (the default), and overdrive speed (the faster gear). The power-on

default is standard speed. The speed of 1-Wire slaves is switched to overdrive using a ROM function command, which is to be transmitted at standard speed. After that, all communication, including the reset/presence-detect cycle, occurs at overdrive speed. The return to standard speed is accomplished through a reset/presence-detect cycle issued at standard speed. Besides commands and data, the 1-Wire bus also delivers power to 1-Wire slave devices that typically do not have a power supply pin. To ensure proper power delivery, the 1-Wire bus must be at V_{CC} level unless communication is taking place.

This section describes the 1-Wire signals as they appear with the DS2483. The figures use different line types and colors to distinguish the various actions.

Write-Zero Time Slot

This time slot (**Figure 2**) consists of two elements: the master pulldown as specified by t_{W0L} and the master pullup as specified by t_{REC0}. Both parameters are configurable. The power-on defaults values (64µs and 5.25µs at standard speed, 8µs and 5µs at overdrive speed) yield a time slot duration of standard 69.25µs (14.4kbps) and overdrive 13.25µs (75.5kbps).

The write-zero low time t_{W0L} can be reduced to 60µs or 6µs if supported by the 1-Wire slaves at the given operating voltage. The write-zero recovery time t_{REC0}, can be reduced to 2.75µs for small networks if active pullup is enabled (APU = 1). This raises the data rate to 15.9kbps (standard) and 114.2kbps (overdrive). Heavily loaded networks may need an extended recovery time. See section *How Many Slaves Can the DS2483 Drive?* for additional information.

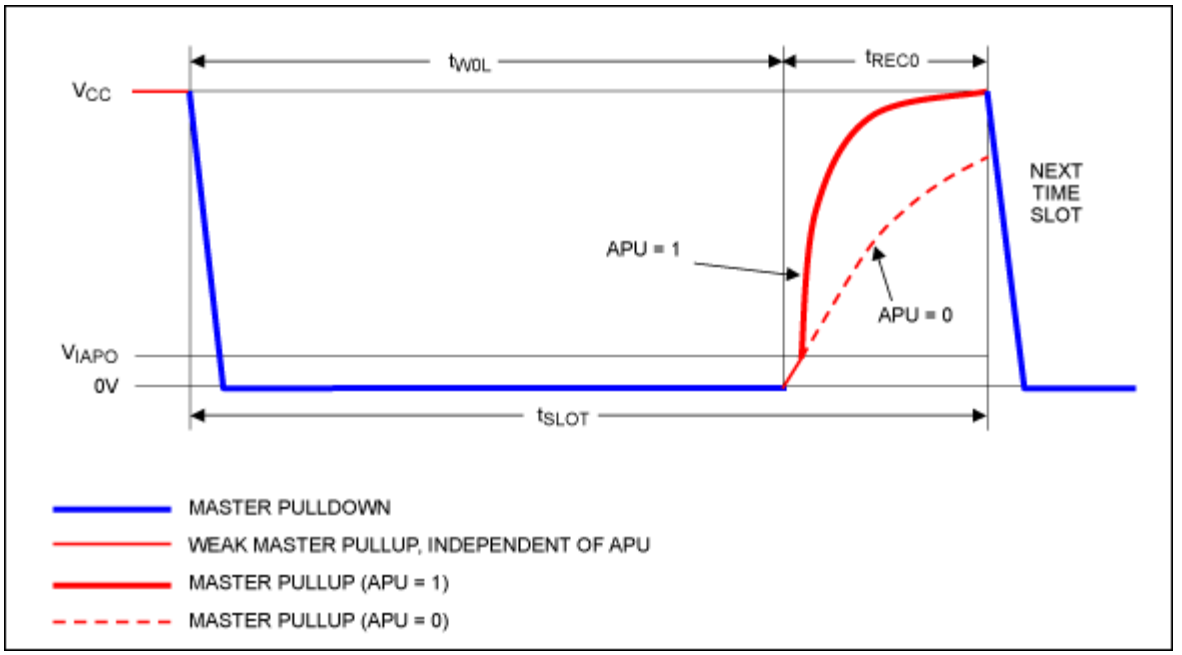

Figure 2. Write-zero time slot.

Write-One/Read-One Time Slot

This time slot (**Figure 3**) consists of two elements: the master pulldown as specified by t_{W1L} and the remainder of the time slot. The master pulldown time is fixed (8µs standard, 0.75µs overdrive). The time slot duration is configurable (equal to t_{W0L} + t_{REC0}). Note that the write-one/read-one time slot delivers a

lot of power to the 1-Wire bus.

At t_{MSR}, the DS2483 samples the voltage on the 1-Wire bus to perform a read operation. The read sample time t_{MSR} is fixed to 12µs (standard) and 1.75µs (overdrive) measured from the beginning of the time slot. This leaves 4µs (standard) and 1.0µs (overdrive) for the voltage to rise to the V_{IH1} threshold, which must be reached to read a 1. If active pullup is enabled (APU = 1) and the voltage does not reach the V_{IH1} level within 1.0µs, the network does not support overdrive speed. For additional information, see section *How Many Slaves Can the DS2483 Drive?*

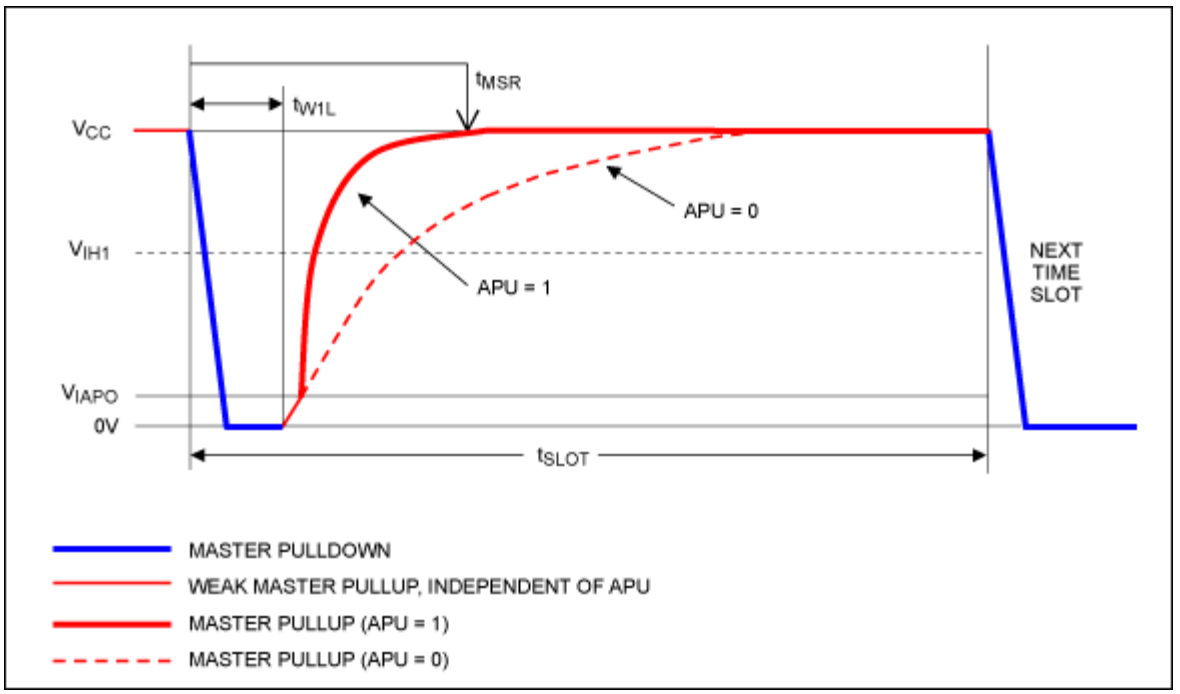

Figure 3. Write-one, read-one time slot.

Read-Zero Time Slot

This time slot (**Figure 4**) consists of three elements: the master pulldown as specified by t_{W1L}; the slave pulldown time; and the remainder of the time slot. The time slot duration is configurable (equal to t_{W0L} + t_{REC0}). The master pulldown time is fixed (8µs standard, 0.75µs overdrive). Note that the read-zero time slot delivers less power than a write-one/read-one time slot.

At t_{MSR}, the DS2483 samples the voltage on the 1-Wire bus to perform a read operation. The read sample time t_{MSR} is fixed to 12µs (standard) and 1.75µs (overdrive) after the beginning of the time slot. The slave pulldown time is slave dependent. Instead of the slave pulldown time, 1-Wire slave data sheets typically specify t_{MSR}. The t_{MSR} timing of the DS2483 is set to meet the requirements of all 1-Wire slaves at standard and almost all slaves at overdrive speed.

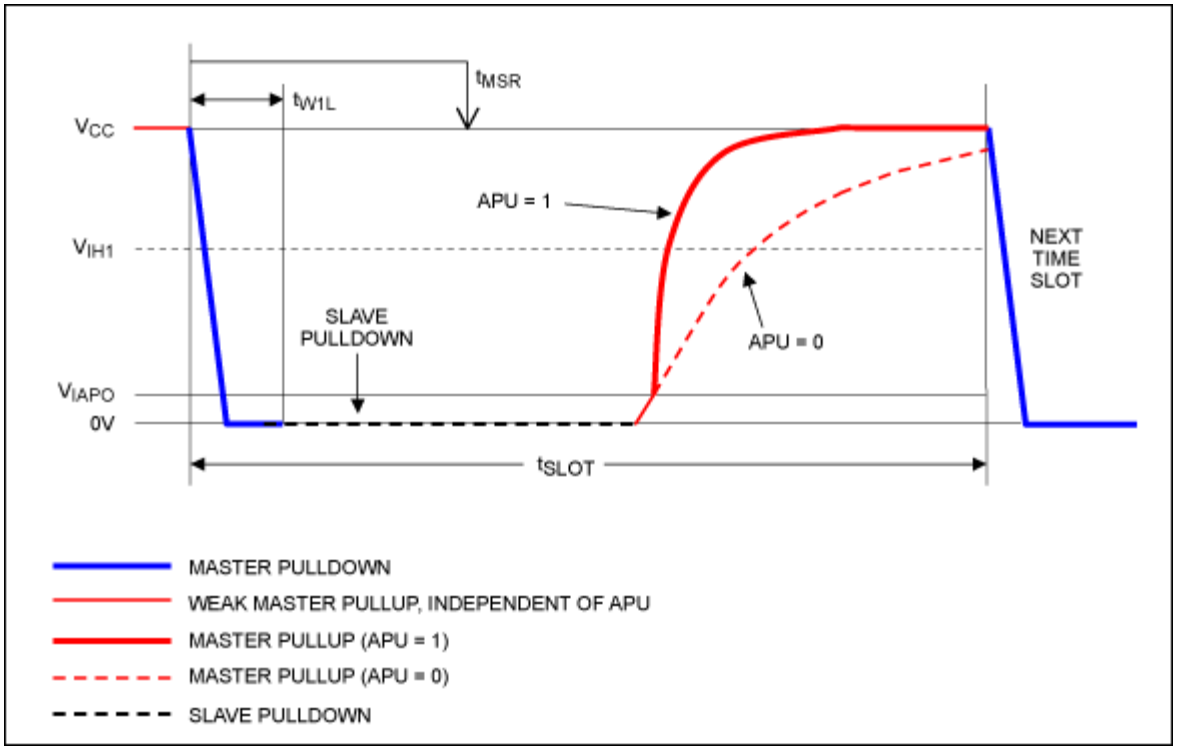

Figure 4. Read-zero time slot.

Reset/Presence-Detect Cycle

This signal (Figure 5) consists of four elements: the master pulldown during the reset-low time t_{RSTL}; the master pullup during t_{PDH}; the subsequent slave pulldown time as specified by t_{PDL}; and the master pullup during the remainder of the cycle. The reset-low time and the reset-high time have the same duration, which is configurable. The power-on defaults are 560µs (standard) and 56µs (overdrive), which yield a default cycle duration of 1120µs and 112µs, respectively. The cycle duration can be reduced to 960µs or 96µs if supported by the 1-Wire slaves at the given operating voltage. A longer cycle time than the default may be needed with some 1-Wire slaves in a low-voltage environment.

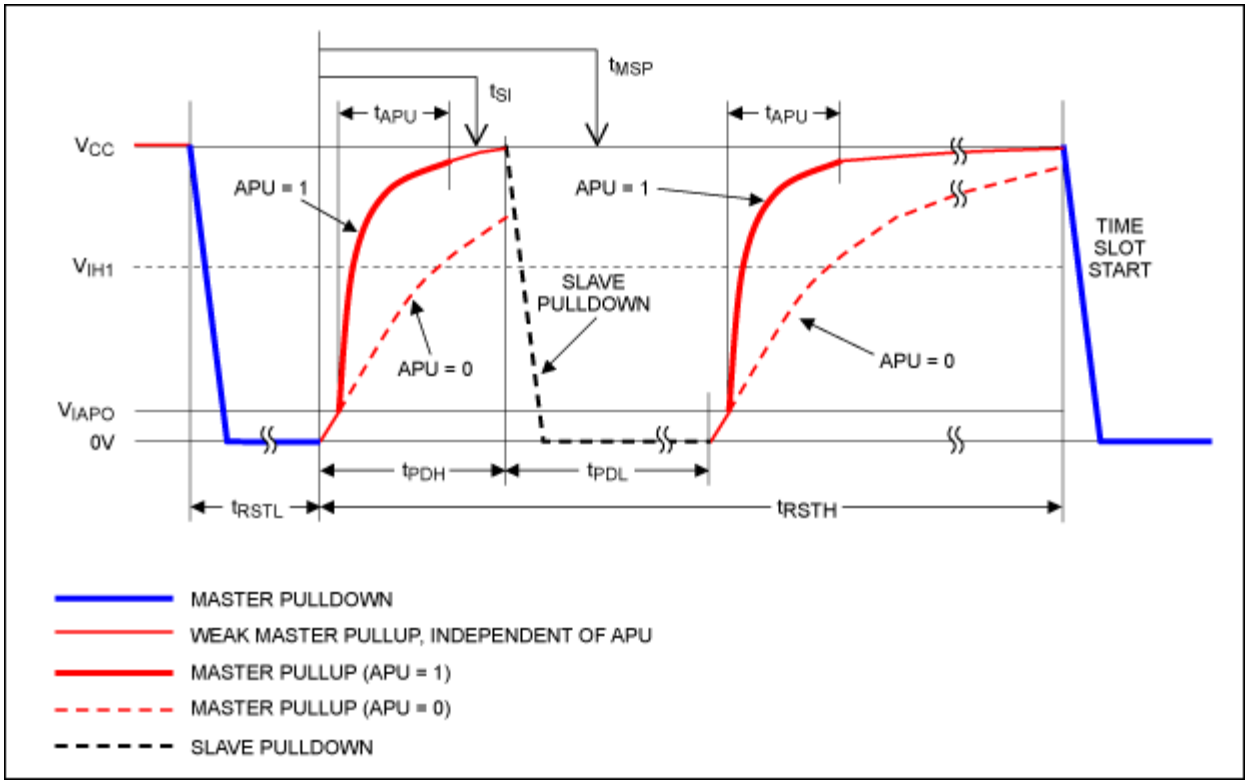

Figure 5. Reset/presence-detect cycle.

The DS2483 samples the voltage on the 1-Wire bus at two instances: t_{SI} to test for a short circuit or interrupt, and at t_{MSP}, to test for a presence pulse generated by one or more 1-Wire slaves on the bus. The sampling time for short or interrupt is fixed to 8µs (standard) and 0.75µs (overdrive) measured from the end of the reset-low time. This leaves 8µs (standard) and 0.75µs (overdrive) for the voltage to rise to the V_{IH1} threshold, which must be reached for the cycle to not report a short circuit on the bus.

The sampling time for the presence pulse t_{MSP} is configurable. The power-on default values are 68µs (standard) and 8µs (overdrive), measured from the end of the reset-low time. These values work for most 1-Wire slaves. An earlier or later sampling point may be necessary for some 1-Wire slaves in a low-voltage environment. The permissible t_{MSP} range is usually specified in the slave data sheets. If not specified, the t_{MSP} minimum is equal to the t_{PDH} maximum; the t_{MSP} maximum is equal to the sum of the t_{PDH} and t_{PDL} minimum values.

In contrast to time slots, the active master pullup (APU = 1) does not start immediately after the V_{IAPO} threshold is crossed; there could be a latency of up to 250ns before the active pullup starts. In addition, to prevent a low-impedance path from V_{CC} to GND when the slave generates a presence pulse, the tAPU duration is very short (overdrive 0.5µs, standard 2.5µs) and ends before the t_{SI} sampling event, after which the weak pullup continues. Therefore, it is highly recommended to enable the active pullup (APU = 1) in the Device Configuration register at either 1-Wire speed. Due to the randomness of the latency, a network may function properly at overdrive speed even if the 1-Wire reset command frequently reports a short circuit (status register bit SD = 1). The short detection is reliable at standard speed.

How Many Slaves Can the DS2483 Drive?

The answer depends on many factors: the operating voltage and configuration settings, the choice or mix of 1-Wire slaves on the bus, the capacitive load imposed by the cable, and—to some extent—even the operating temperature.

For the DS2483, it is possible to create a mathematical model that describes the voltage as it rises when the master (or slave) stops pulling the bus low. This changes the question to: Can the DS2483 drive my network? As shown below, this question can be answered using some mathematics.

First Order Model of a 1-Wire Slave

A typical parasitically powered 1-Wire slave can be described as a capacitor with two ranges: low capacitance and high capacitance. The transition from low to high takes place at a voltage called V_{SRKI}, where the slave recharge kicks in. In addition, 1-Wire slaves have a leakage current. This results in the following list of parameters to describe the slave (**Table 2**).

Table 2. Slave Parameter Descriptions

Parameter Symbol	Description	Numeric Value/Source
C_{SLOW}	Slave low capacitance	50pF, usually not specified in data sheets.
C_{SHIGH}	Slave high capacitance	600pf to 1500pF typical, see slave data sheet. For V_{CC}-powered 1-Wire slaves, the C_{SLOW} value also applies for C_{SHIGH}.
V_{SRKI}	Range transition voltage	Ca. 50% of supply voltage or 1.3V, whatever is higher; not electrically measurable.
I_L	Leakage current	5µA to 10µA typical, see slave data sheet.

The impact of the leakage current is minimal, unless the network has a large number of slaves. For a multislave network, the slave capacitance and leakage current must be multiplied by the number of slaves or added up if the slaves are of different types.

First Order Model of the DS2483 Master Port

Besides the operating voltage, the master port (Figure 1) is described by the weak pullup resistance (configurable), the active pullup resistance, the threshold at which the active pullup starts (if enabled), and the threshold that needs to be reached for the voltage on the 1-Wire bus to be read as logic 1. This results in the following list of parameters to describe the master (**Table 3**).

Table 3. Master Parameter Descriptions		
Parameter Symbol	**Description**	**Numeric Value/Source**
R_{WPU}	Resistor responsible for weak master pullup, red line in the figure legends or dotted red line (APU = 0)	500Ω or 1000Ω typically, see data sheet for tolerance.
R_{APU}	Resistor responsible for active master pullup, bold red line in the figure legends	100Ω or less, depends on supply voltage, see data sheet.
V_{IAPO}	Threshold voltage at which the active pullup starts, if APU = 1	0.95V typically, see data sheet.
V_{IH1}	1-Wire input high voltage	60% of V_{CC}, see data sheet.

First Order Model of the 1-Wire Network

For a network that extends beyond a circuit board, category 5 phone cable is recommended. Such cables have a typical capacitance on 50pF/meter between the wires of a twisted pair. The cable has a characteristic impedance of 100Ω to 110Ω, which becomes relevant if the cable extends beyond ca. 50 meters in length.

Definitions and Preparations (APU = 1)

Figure 6 shows the recharge curve of a time slot at a magnified scale. The recharge consists of three sections: S1, S2, and S3. Section S1 begins when the pulldown (master or slave) ends and the 1-Wire bus starts to recharge through R_{WPU}. S1 ends when the V_{IAPO} threshold is crossed. Section S2 starts when S1 ends and stops when V_{SRKI} is crossed. Section S3 begins when S2 ends and stops at the end of the time slot.

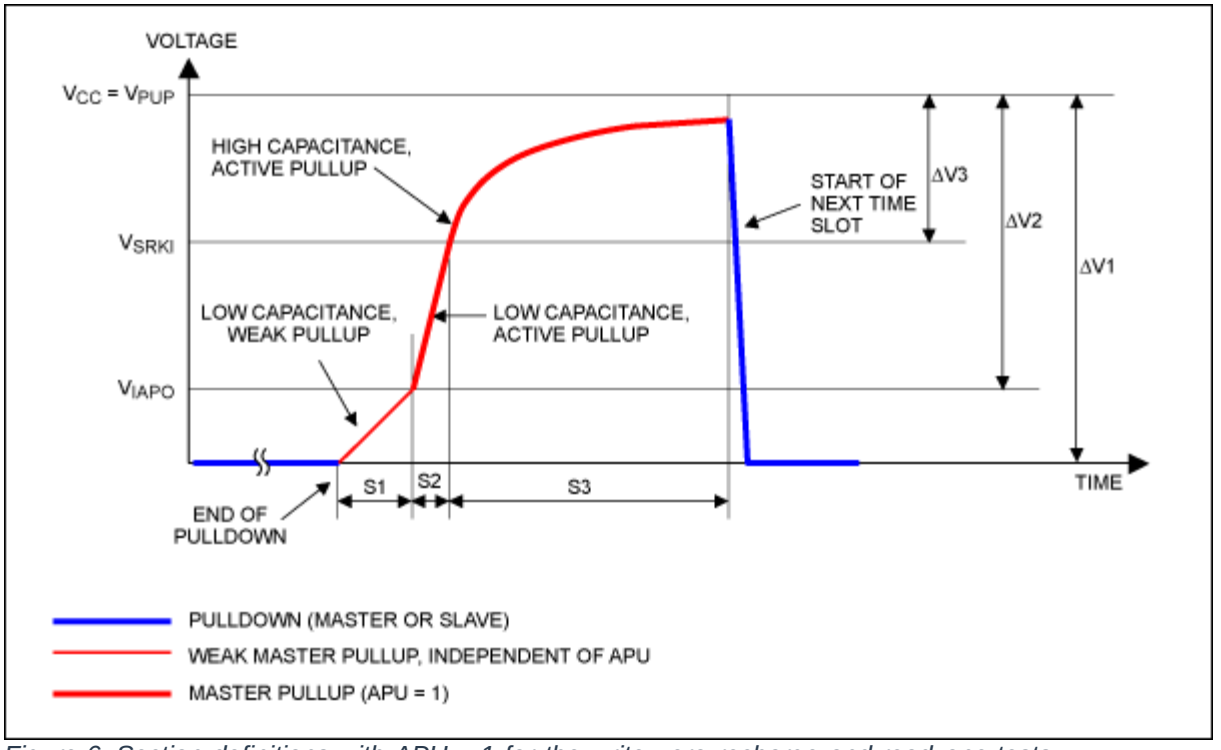

Figure 6. Section definitions with APU = 1 for the write-zero recharge and read-one tests.

Section S1 is governed by R_{WPU}, the low capacitance, and the initial voltage difference of ΔV1. During section S2, R_{APU} applies together with the low capacitance and an initial voltage difference of ΔV2. For section 3 we are dealing with R_{APU}, the high capacitance, and the initial voltage difference of ΔV3.

The initial voltage differences are calculated using Equations 1 to 3.

$$\Delta V1 = V_{CC} - R_{WPU} \times (\text{number of slaves}) \times I_L \quad \text{(Eq. 1)}$$

$$\Delta V2 = V_{CC} - V_{IAPO} - R_{APU} \times (\text{number of slaves}) \times I_L \quad \text{(Eq. 2)}$$

$$\Delta V3 = V_{CC} - V_{SRKI} - R_{APU} \times (\text{number of slaves}) \times I_L \quad \text{(Eq. 3)}$$

To calculate the applicable capacitance values, use Equations 4 and 5.

$$C_{LOW} = (\text{number of slaves}) \times C_{SLOW} + (\text{cable capacitance}) \quad \text{(Eq. 4)}$$

$$C_{HIGH} = (\text{number of slaves}) \times C_{SHIGH} + (\text{cable capacitance}) \quad \text{(Eq. 5)}$$

Use Equations 6 and 7 to calculate the duration of sections S1 and S2.

$$S1 = -1 \times R_{WPU} \times C_{LOW} \times \ln(1 - V_{IAPO}/\Delta V1) \quad \text{(Eq. 6)}$$

$$S2 = -1 \times R_{APU} \times C_{LOW} \times \ln[1 - (V_{SRKI} - V_{IAPO})/\Delta V2] \quad \text{(Eq. 7)}$$

Write-Zero Recharge Test

For the given V_{CC}, number of slaves and cable capacitance, starting with the DS2483 default configuration and setting APU = 1, calculate the duration of S1 and S2.

If S1 + S2 > 5.25µs (t_{REC0} default value), the load is too high. Increase t_{REC0} and/or select the low R_{WPU} value.

Calculate S3, the duration of section 3, using Equation 8.

$$S3 = t_{REC0} - S1 - S2 \quad \text{(Eq. 8)}$$

Now calculate the voltage increase during section 3 using Equation 9.

$$V_{S3} = \Delta V3 \times (1 - EXP[-1 \times S3/(R_{APU} \times C_{HIGH})]) \quad \text{(Eq. 9)}$$

If the $V_{S3} + V_{SRKI}$ is reasonably high, e.g., 80% to 90% of V_{CC}, the network has passed the write-zero recharge test. Otherwise, increase t_{REC0} by another 2.5µs and repeat the calculation. To see the difference between APU = 1 and APU = 0, repeat the calculations above, substituting R_{APU} with R_{WPU}. The network will fail unless you increase t_{REC0} close to its limit.

Passing this test is important to ensure that the slaves have enough energy stored to survive a long series of write-zero time slots. The network can still fail the read-one test.

Read-One Test

For this test one must distinguish two cases: $V_{SRKI} < V_{IH1}$ and $V_{SRKI} > V_{IH1}$.

Case 1: $V_{SRKI} < V_{IH1}$

Step 1

Take the S1 and S2 values from the write-zero recharge test. If S1 + S2 is larger than 1.0µs (= overdrive t_{MSR} - overdrive t_{W1L}), the test failed for overdrive speed. If S1 + S2 is larger than 4µs (= standard t_{MSR} - standard t_{W1L}), the test also failed for standard speed. See section *What Can I Do If the Tests Fail at Standard Speed?* for recommendations.

Step 2

If Step 1 is passed, calculate how deep into S3 the read sampling takes place, for both speeds.

$$S3_{RO} = 1.0\mu s - S1 - S2 \quad \text{(Eq. 10a)}$$

$$S3_{RS} = 4\mu s - S1 - S2 \quad \text{(Eq. 10b)}$$

Next, for the passing speed(s), calculate the voltage increase from the beginning of S3 to the sampling points $S3_{RO}$ and $S3_{RS}$, respectively.

$$V \quad = \Delta V3 \times (1 - EXP[-1 \times S3 \quad /(R \quad \times C \quad)]) \quad \text{(Eq. 11a)}$$

RS3O RO APU HIGH

$$V_{RS3S} = \Delta V3 \times (1 - EXP[-1 \times S3_{RS}/(R_{APU} \times C_{HIGH})]) \quad \text{(Eq. 11b)}$$

If $V_{RS3O} + V_{SRKI}$ is larger than V_{IH1}, the test is passed for overdrive. The network will also work at standard speed. If this test failed, check whether $V_{RS3S} + V_{SRKI}$ is larger than V_{IH1}. If this test is passed, the network will work at standard speed, but not at overdrive.

Case 2: $V_{SRKI} > V_{IH1}$

Take the S1 value from the write-zero recharge test. Then calculate how deep into S2 the read sampling takes place.

$$S2_R = -1 \times R_{APU} \times C_{LOW} \times \ln[1 - (V_{IH1} - V_{IAPO})/\Delta V2] \quad \text{(Eq. 12)}$$

If $S1 + S2_R$ is larger than 1.0µs, the test failed for overdrive. If $S1 + S2_R$ is less than 4µs, the test is passed for standard speed. Otherwise, the load is too high even for standard speed. In this case see section *What Can I Do If the Tests Fail at Standard Speed?* for recommendations.

The t_{SI} sampling at standard speed is passed automatically if the read-one test is passed at standard speed. As explained in the Reset/Presence-Detect Cycle section, the t_{SI} sampling at overdrive speed does not provide reliable results. Therefore, the short/interrupt test—if implemented in the application software—should be performed at standard speed.

Numerical Example

Parameter	Value
V_{CC}	3.3V
C_{SLOW}	50pF
C_{SHIGH}	800pF
C_{CABLE}	1000pF (20m)
I_L	10µA
V_{IAPO}	1.2V
R_{WPU}	1000Ω
R_{APU}	60Ω
V_{SRKI}	1.65V (50% of V_{CC})
t_{REC0}	5.25µs
Recharge threshold	90% of V_{CC}
V_{IH1}	1.98V
#slaves	10

Preparation

$V_{IH1} = 0.6 \times V_{CC}$ = 1.98V

$\Delta V1 = V_{CC} - R_{WPU} \times (\text{number of slaves}) \times I_L$ = 3.2V

$\Delta V2 = V_{CC} - V_{IAPO} - R_{APU} \times (\text{number of slaves}) \times I_L$ = 2.094V

$\Delta V3 = V_{CC} - V_{SRKI} - R_{APU} \times (\text{number of slaves}) \times I_L$ = 1.644

$C_{LOW} = (\text{number of slaves}) \times C_{SLOW} + (\text{cable capacitance})$ = 1500pF

$C_{HIGH} = (\text{number of slaves}) \times C_{SHIGH} + (\text{cable capacitance})$ = 9000pF

$S1 = -1 \times R_{WPU} \times C_{LOW} \times \ln(1 - V_{IAPO}/\Delta V1)$ = 0.705µs

$S2 = -1 \times R_{APU} \times C_{LOW} \times \ln[1 - (V_{SRKI} - V_{IAPO})/\Delta V2]$ = 0.0218µs

Write-Zero Recharge Test

$S3 = t_{REC0} - S1 - S2$ = 4.523µs

$V_{S3} = \Delta V3 \times (1 - \text{EXP}[-1 \times S3/(R_{APU} \times C_{HIGH})])$ = 1.644V

$V_{S3END} = V_{SRKI} + V_{S3}$ = 3.294V

V_{S3END} > 2.97V (90% of V_{CC}); **passed**.

Read-One Test

Case 1: $V_{SRKI} < V_{IH1}$

Step 1

S1 + S2 = 0.7268µs < 1.0µs: **passed for overdrive speed**.
S1 + S2 = 0.7268µs < 4µs; **passed for standard speed**.

Step 2

$S3_{RO} = 1.0\mu s - S1 - S2$ = 0.273µs

$V_{RS3O} = \Delta V3 \times (1 - \text{EXP}[-1 \times S3_{RO}/(R_{APU} \times C_{HIGH})])$ = 0.653V

0.653V + 1.65V = 2.303V > 1.98V; **passed for overdrive speed**.

$S3_{RS} = 4\mu s - S1 - S2$ = 3.273µs

$V_{RS3S} = \Delta V3 \times (1 - \text{EXP}[-1 \times S3_{RS}/(R_{APU} \times C_{HIGH})])$ = 1.640V

1.640V + 1.65V = 3.29V > 1.98V; **passed for standard speed**.

Since $V_{SRKI} < V_{IH1}$, Case 2 does not apply.

What Can I Do If the Tests Fail at Standard Speed?

Generally, the number of slaves that a master can drive grows with the supply voltage, V_{CC}. If the network fails at 3.3V, chances are that it will work at 5V. If the load is still too high, split the network into smaller networks, using electronic switches to operate one small network at a time, as shown in tutorial

148, "Guidelines for Reliable Long Line 1-Wire Networks." Since the read sampling time t_{MSR} is fixed at 12µs, the DS2483 cannot compensate for signal propagation delays that occur with long cables, e.g., 100m or more. For such applications, the DS2480B master is the better choice, though not perfect. The ultimate driver for long lines is featured in reference design 244, "Advanced 1-Wire Network Driver."

Summary

The DS2483 represents the next generation of integrated 1-Wire masters. Functionally, the device offers the convenience of the DS2482 together with a load-handling capability similar to the DS2480B. With its configurability, the 2-stage power-savings mode, and the level translator function, the DS2483 is well suited for battery-operated applications. This application note explains the operation of the 1-Wire master port, gives advice on when to deviate from the default configurations, and explains how to determine the drive capability for a given network. The mathematical model presented to test the drive capability can be downloaded as an Excel® spreadsheet.

Related Parts		
DS2480B	Serial to 1-Wire Line Driver	Free Samples
DS2482-100	Single-Channel 1-Wire Master	Free Samples
DS2482-101	Single-Channel 1-Wire® Master with Sleep Mode	Free Samples
DS2482-800	8-Channel 1-Wire Master	Free Samples
DS2483	Single-Channel 1-Wire Master with Adjustable Timing and Sleep Mode	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 5273: http://www.maximintegrated.com/an5273
APPLICATION NOTE 5273, AN5273, AN 5273, APP5273, Appnote5273, Appnote 5273