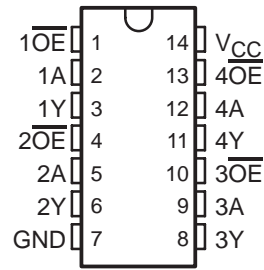


SN64BCT125A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCBS052B – JULY 1990 – REVISED MAY 1994

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- High-Impedance State During Power-Up and Power-Down
- 3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)

D OR N PACKAGE
(TOP VIEW)



description

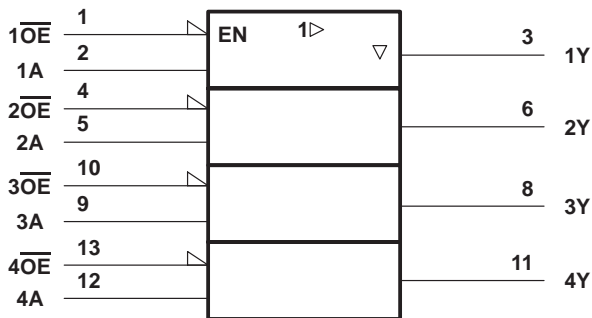
The SN64BCT125A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

The SN64BCT125A is characterized for operation from -40°C to 85°C and 0°C to 70°C .

FUNCTION TABLE
(each buffer)

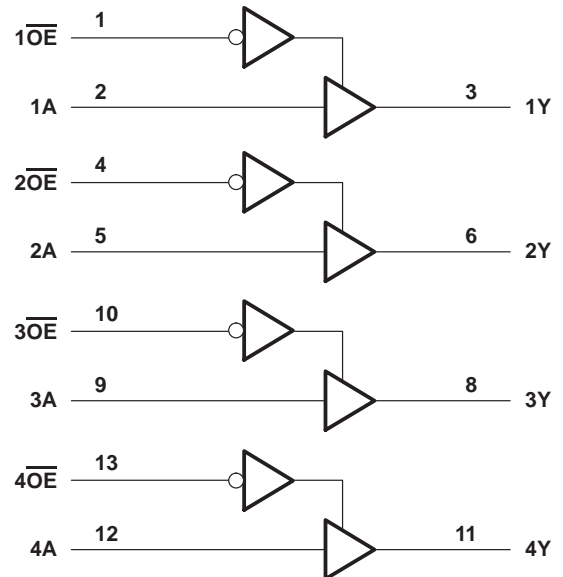
INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN64BCT125A

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	– 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	– 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	– 0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	– 40°C to 85°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{IK} Input clamp current			–18	mA
I_{OH} High-level output current			–15	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.3		V
		$I_{OH} = -15$ mA	2	3.1		
V_{OL}	$V_{CC} = 4.5$ V,	$I_{OH} = 64$ mA		0.42	0.55	V
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50	μA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			–50	μA
I_{OZ}	$V_{CC} = 0$ to 1.3 V (power up)	$V_O = 2.7$ V or 0.5 V, \overline{OE} at 0.8 V			± 50	μA
	$V_{CC} = 1.3$ V to 0 (power down)				± 50	
I_I	$V_{CC} = 0$,	$V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			25	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V			–20	μA
$I_{OS}§$	$V_{CC} = 5.5$ V,	$V_O = 0$	–100		–225	mA
I_{CCL}	$V_{CC} = 5.5$ V			46	49	mA
I_{CCH}	$V_{CC} = 5.5$ V			19	31	mA
I_{CCZ}	$V_{CC} = 5.5$ V			6	14	mA
C_i	$V_{CC} = 5$ V,	$V_I = 2.5$ V or 0.5 V		4		pF
C_o	$V_{CC} = 5$ V,	$V_O = 2.5$ V or 0.5 V		9		pF

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



SN64BCT125A
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

SCBS052B – JULY 1990 – REVISED MAY 1994

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
						T _A = -40°C to 85°C		T _A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t _{PHL}			2.7	5	6.9	2.7	8	2.7	7.7	
t _{PZH}	$\overline{\text{OE}}$	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t _{PZL}			5	8.2	10.4	5	12.8	5	11.7	
t _{PHZ}	$\overline{\text{OE}}$	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t _{PLZ}			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN64BCT125AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT125A	Samples
SN64BCT125AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN64BCT125AN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE




*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN64BCT125AD	D	SOIC	14	50	506.6	8	3940	4.32
SN64BCT125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN64BCT125AN	N	PDIP	14	25	506	13.97	11230	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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