Ultra-Tiny, Differential, 16-Bit ΔΣ ADC with SPI Interface

FEATURES

- **$\pm V_{CC}$ Differential Input Range**
- **16-Bit Resolution (Including Sign), No Missing Codes**
- **2LSB Offset Error**
- **4LSB Full-Scale Error**
- **60 Conversions Per Second**
- Single Conversion Settling Time for Multiplexed Applications
- Single-Cycle Operation with Auto Shutdown
- 800µA Supply Current
- 0.2µA Sleep Current
- Internal Oscillator—No External Components Required
- SPI Interface
- Ultra-Tiny 3mm × 2mm DFN and TSOT-23 Packages

APPLICATIONS

- System Monitoring
- Environmental Monitoring
- Direct Temperature Measurements
- Instrumentation
- Industrial Process Control
- Data Acquisition
- Embedded ADC Upgrades

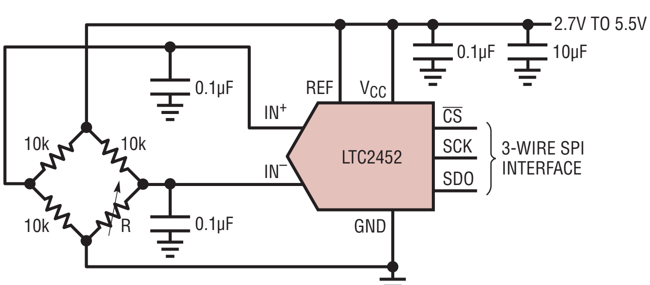
DESCRIPTION

The LTC®2452 is an ultra-tiny, fully differential, 16-bit, analog-to-digital converter. The LTC2452 uses a single 2.7V to 5.5V supply and communicates through an SPI interface. The ADC is available in an 8-pin, 3mm × 2mm DFN package or TSOT-23 package. It includes an integrated oscillator that does not require any external components. It uses a delta-sigma modulator as a converter core and has no latency for multiplexed applications. The LTC2452 includes a proprietary input sampling scheme that reduces the average input sampling current several orders of magnitude when compared to conventional delta-sigma converters. Additionally, due to its architecture, there is negligible current leakage between the input pins.

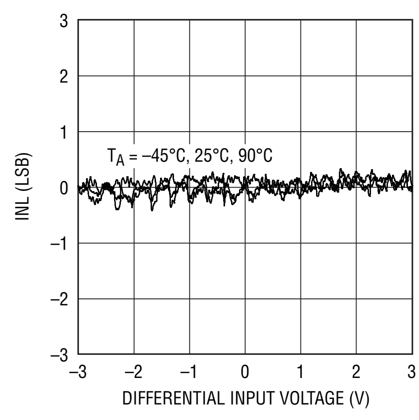
The LTC2452 can sample at 60 conversions per second, and due to the very large oversampling ratio, has extremely relaxed anti-aliasing requirements. The LTC2452 includes continuous internal offset and full-scale calibration algorithms which are transparent to the user, ensuring accuracy over time and over the operating temperature range. The converter has an external REF pin and the differential input voltage range can extend up to $\pm V_{REF}$.

Following a single conversion, the LTC2452 can automatically enter a sleep mode and reduce its supply current to less than 0.2µA. If the user reads the ADC once a second, the LTC2452 consumes an average of less than 50µW from a 2.7V supply.

TYPICAL APPLICATION



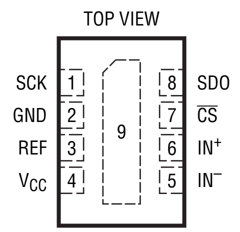
Integral Nonlinearity, V_{CC} = 3V



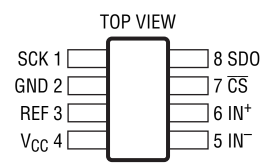
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) .... –0.3V to 6V
Analog Input Voltage (V_{IN}^+, V_{IN}^-) . –0.3V to (V_{CC} + 0.3V)
Reference Voltage (V_{REF}) .... –0.3V to (V_{CC} + 0.3V)
Digital Voltage (V_{SDO}, V_{SCK}, $V_{\overline{CS}}$) . –0.3V to (V_{CC} + 0.3V)
Storage Temperature Range .... –65°C to 150°C
Operating Temperature Range
LTC2452C .... 0°C to 70°C
LTC2452I .... –40°C to 85°C

PIN CONFIGURATION



DD8 PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
C/I GRADE T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
C/I GRADE T_{JMAX} = 125°C, θ_{JA} = 140°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2452CDDB#TRMPBF	LTC2452CDDB#TRPBF	LDNJ	8-Lead Plastic (3mm × 2mm) DFN	0°C to 70°C
LTC2452IDDB#TRMPBF	LTC2452IDDB#TRPBF	LDNJ	8-Lead Plastic (3mm × 2mm) DFN	–40°C to 85°C
LTC2452CTS8#TRMPBF	LTC2452CTS8#TRPBF	LTDPK	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2452ITS8#TRMPBF	LTC2452ITS8#TRPBF	LTDPK	8-Lead Plastic TSOT-23	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	(Note 3)	●	16			Bits
Integral Nonlinearity	(Note 4)	●		1	10	LSB
Offset Error		●		2	10	LSB
Offset Error Drift				0.02		LSB/°C
Gain Error		●		0.01	0.02	% of FS
Gain Error Drift				0.02		LSB/°C
Transition Noise				2.2		μV_{RMS}
Power Supply Rejection DC				80		dB

2452fd

ANALOG INPUTS AND REFERENCES

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Positive Input Voltage Range		●	0		V_{REF}	V
V_{IN}^-	Negative Input Voltage Range		●	0		V_{REF}	V
V_{REF}	Reference Voltage Range		●	2.5		V_{CC}	V
$V_{OR}^+ + V_{UR}^+$	Overrange + Underrange Voltage, IN+	V_{REF} = 5V, V_{IN}^- = 2.5V (See Figure 3)			31		LSB
$V_{OR}^- + V_{UR}^-$	Overrange + Underrange Voltage, IN–	V_{REF} = 5V, V_{IN}^+ = 2.5V (See Figure 3)			31		LSB
C_{IN}	IN+, IN– Sampling Capacitance				0.35		pF
$I_{DC\_LEAK(IN^+)}$	IN+ DC Leakage Current	V_{IN} = GND (Note 10) V_{IN} = V_{CC} (Note 10)	● ●	–10 –10	1 1	10 10	nA nA
$I_{DC\_LEAK(IN^-)}$	IN– DC Leakage Current	V_{IN} = GND (Note 10) V_{IN} = V_{CC} (Note 10)	● ●	–10 –10	1 1	10 10	nA nA
$I_{DC\_LEAK(REF)}$	REF DC Leakage Current	V_{REF} = 3V (Note 10)	●	–10	1	10	nA
I_{CONV}	Input Sampling Current (Note 5)				50		nA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Sleep	 $\overline{CS}$ = GND (Note 6) $\overline{CS}$ = V_{CC} (Note 6)	 ● ●		 800 0.2	 1200 0.6	 µA µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range,otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	V_{CC} – 0.3			V
V_{IL}	Low Level Input Voltage		●			0.3	V
I_{IN}	Digital Input Current		●	–10		10	µA
C_{IN}	Digital Input Capacitance				10		pF
V_{OH}	High Level Output Voltage	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage Current		●	–10		10	µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time		●	13	16.6	23	ms
f_{SCK}	SCK Frequency Range		●			2	MHz
t_{lSCK}	SCK Low Period		●	250			ns
t_{hSCK}	SCK High Period		●	250			ns
t_1	$\overline{CS}$ Falling Edge to SDO Low-Z	(Notes 7, 8)	●	0		100	ns
t_2	$\overline{CS}$ Rising Edge to SDO Hi-Z	(Notes 7, 8)	●	0		100	ns
t_3	$\overline{CS}$ Falling Edge to SCK Falling Edge		●	100			ns
t_{KQ}	SCK Falling Edge to SDO Valid	(Note 7)	●	0		100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltage values are with respect to GND. V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REFCM} = V_{REF}/2$, $FS = V_{REF}$

$V_{IN} = V_{IN}^+ – V_{IN}^–$, $–V_{REF} \le V_{IN} \le V_{REF}$; $V_{INCM} = (V_{IN}^+ + V_{IN}^–)/2$.

Note 3. Guaranteed by design, not subject to test.

Note 4. Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. Guaranteed by design and test correlation.

Note 5: $\overline{CS} = V_{CC}$. A positive current is flowing into the DUT pin.

Note 6: SCK = V_{CC} or GND. SDO is high impedance.

Note 7: See Figure 4.

Note 8: See Figure 5.

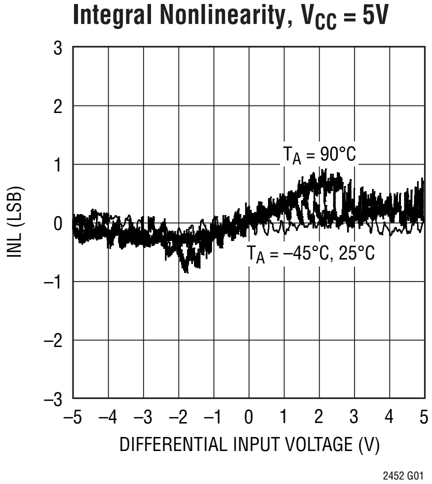
Note 9: Input sampling current is the average input current drawn from the input sampling network while the LTC2452 is actively sampling the input.

Note 10: A positive current is flowing into the DUT pin.

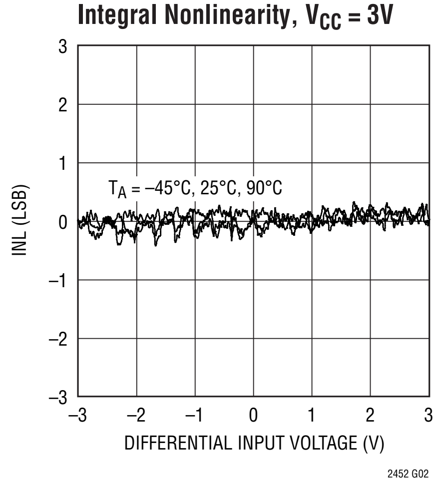
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise noted)

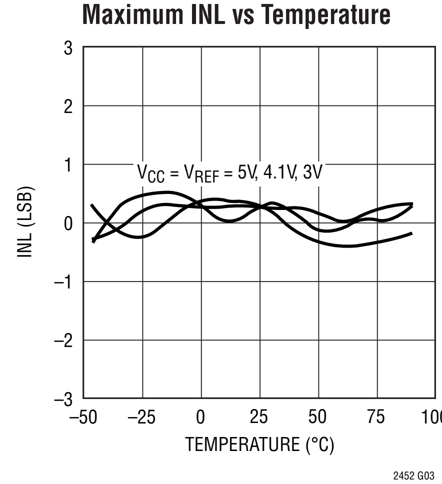
Integral Nonlinearity, V_{CC} = 5V



Integral Nonlinearity, V_{CC} = 3V

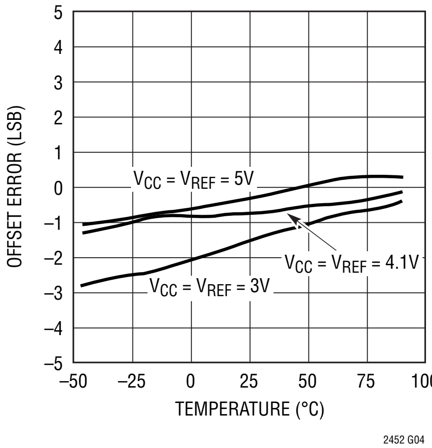


Maximum INL vs Temperature

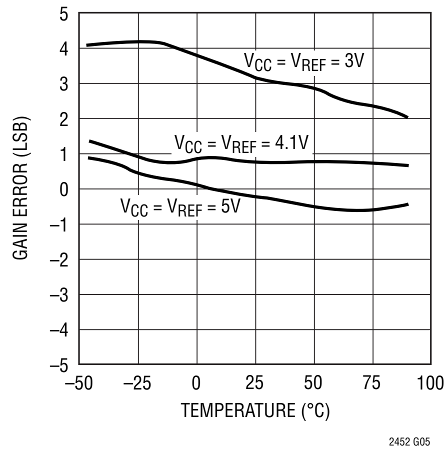


TYPICAL PERFORMANCE CHARACTERISTICS (T$_A$ = 25°C, unless otherwise noted)

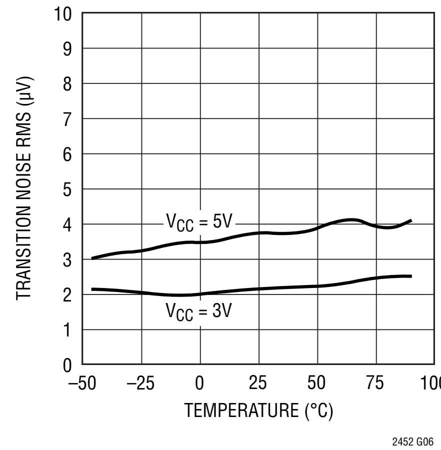
Offset Error vs Temperature



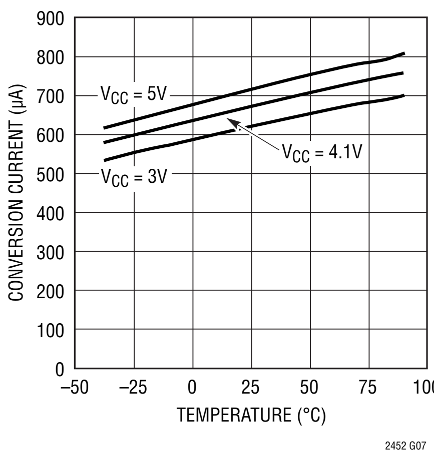
Gain Error vs Temperature



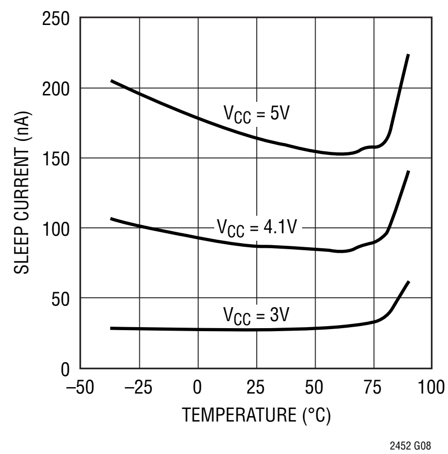
Transition Noise vs Temperature



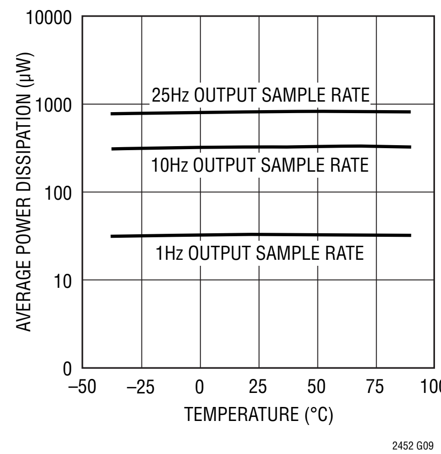
Conversion Mode Power Supply Current vs Temperature



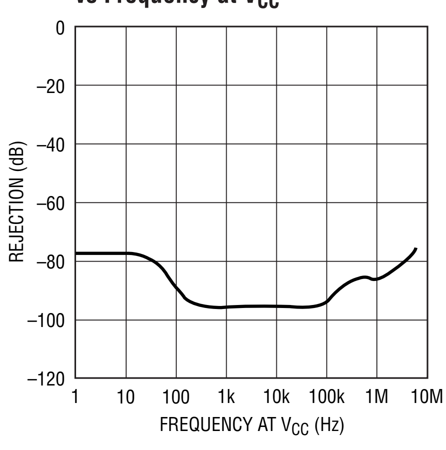
Sleep Mode Power Supply Current vs Temperature



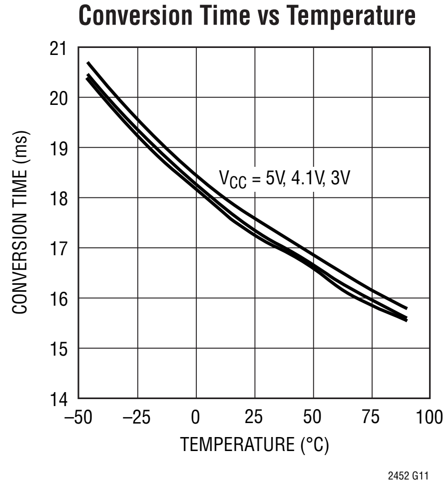
Average Power Dissipation vs Temperature, V_{CC} = 3V



Power Supply Rejection vs Frequency at V_{CC}



Conversion Time vs Temperature



PIN FUNCTIONS

SCK (Pin 1): Serial Clock Input. SCK synchronizes the serial data output. While digital data is available (the ADC is not in CONVERT state) and $\overline{CS}$ is LOW (ADC is not in SLEEP state) a new data bit is produced at the SDO output pin following every falling edge applied to the SCK pin.

GND (Pin 2): Ground. Connect to a ground plane through a low impedance connection.

REF (Pin 3): Reference Input. The voltage on REF can have any value between 2.5V and V_{CC}. The reference voltage sets the full-scale range.

V_{CC} (Pin 4): Positive Supply Voltage. Bypass to GND (Pin 2) with a 10µF capacitor in parallel with a low-series-inductance 0.1µF capacitor located as close to the LTC2452 as possible.

IN^- (Pin 5), IN^+ (Pin 6): Differential Analog Input.

$\overline{CS}$ (Pin 7): Chip Select (Active LOW) Digital Input. A LOW on this pin enables the SDO digital output. A HIGH on this pin places the SDO output pin in a high impedance state.

SDO (Pin 8): Three-State Serial Data Output. SDO is used for serial data output during the DATA OUTPUT state and can be used to monitor the conversion status.

Exposed Pad (Pin 9): Ground. Must be soldered to PCB ground. For prototyping purposes, this pad may remain floating.

BLOCK DIAGRAM

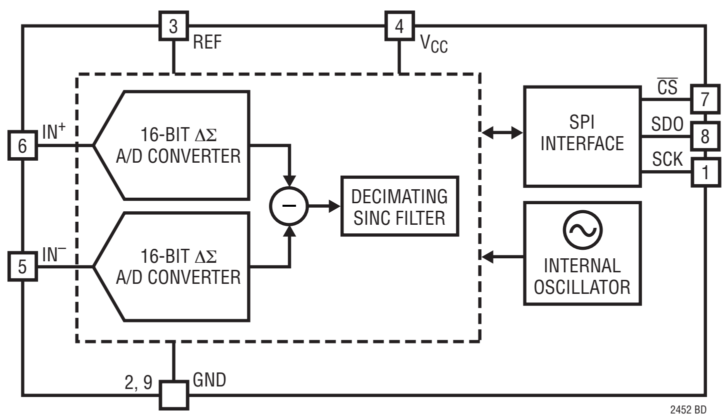


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2452 is a low power, fully differential, delta-sigma analog-to-digital converter with a simple 3-wire SPI interface (see Figure 1). Its operation is composed of three successive states: CONVERT, SLEEP and DATA OUTPUT.

The operating cycle begins with the CONVERT state, is followed by the SLEEP state, and ends with the DATA OUTPUT state (see Figure 2). The 3-wire interface consists of serial data output (SDO), serial clock input (SCK), and the active low chip select input ($\overline{CS}$).

The CONVERT state duration is determined by the LTC2452 conversion time (nominally 16.6 milliseconds). Once

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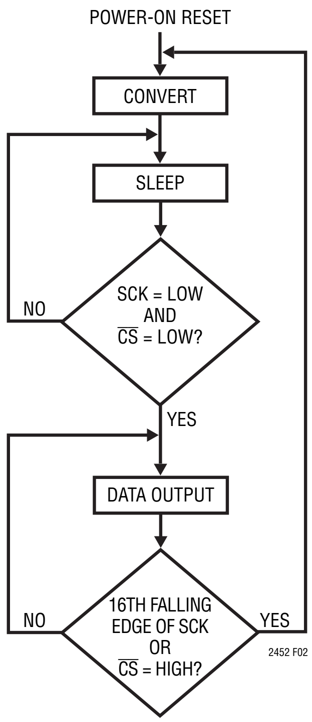

Figure 2. LTC2452 State Transition Diagram

started, this operation can not be aborted except by a low power supply condition (V_{CC} < 2.1V) which generates an internal power-on reset signal.

After the completion of a conversion, the LTC2452 enters the SLEEP state and remains there until both the chip select and serial clock inputs are low ($\overline{CS}$ = SCK = LOW). Following this condition, the ADC transitions into the DATA OUTPUT state.

While in the SLEEP state, whenever the chip select input is pulled high ($\overline{CS}$ = HIGH), the LTC2452's power supply current is reduced to less than 200nA. When the chip select input is pulled low ($\overline{CS}$ = LOW), and SCK is maintained at a HIGH logic level, the LTC2452 will return to a normal power consumption level. During the SLEEP state, the result of the last conversion is held indefinitely in a static register.

Upon entering the DATA OUTPUT state, SDO outputs the sign (D15) of the conversion result. During this state, the ADC shifts the conversion result serially through the SDO output pin under the control of the SCK input pin. There is no latency in generating this data and the result corresponds to the last completed conversion. A new bit of data appears at the SDO pin following each falling edge detected at the SCK input pin and appears from MSB to LSB. The user can reliably latch this data on every rising edge of the external serial clock signal driving the SCK pin (see Figure 3).

The DATA OUTPUT state concludes in one of two different ways. First, the DATA OUTPUT state operation is completed once all 16 data bits have been shifted out and the clock then goes low. This corresponds to the 16th falling edge of SCK. Second, the DATA OUTPUT state can be aborted at any time by a LOW-to-HIGH transition on the $\overline{CS}$ input. Following either one of these two actions, the LTC2452 will enter the CONVERT state and initiate a new conversion cycle.

Power-Up Sequence

When the power supply voltage (V_{CC}) applied to the converter is below approximately 2.1V, the ADC performs a power-on reset. This feature guarantees the integrity of the conversion result.

When V_{CC} rises above this critical threshold, the converter generates an internal power-on reset (POR) signal for approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2452 starts a conversion cycle and follows the succession of states shown in Figure 2. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage V_{CC} is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Ease of Use

The LTC2452 data output has no latency, filter settling delay or redundant results associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog input voltages requires no special actions.

The LTC2452 performs offset calibrations every conversion. This calibration is transparent to the user and has no effect upon the cyclic operation described previously. The advantage of continuous calibration is stability of the ADC performance with respect to time and temperature.

The LTC2452 includes a proprietary input sampling scheme that reduces the average input current by several orders

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of magnitude when compared to traditional delta-sigma architectures. This allows external filter networks to interface directly to the LTC2452. Since the average input sampling current is 50nA, an external RC lowpass filter using 1kΩ and 0.1µF results in <1LSB additional error. Additionally, there is negligible leakage current between IN^+ and $IN^–$.

Reference Voltage Range

The LTC2453 reference input range is 2.5V to V_{CC}. For the simplest operation, REF can be shorted to V_{CC}.

Input Voltage Range

As mentioned in the Output Data Format section, the output code is given as 32768 • V_{IN}/V_{REF} + 32768. For $V_{IN} \ge V_{REF}$, the output code is clamped at 65535 (all ones). For $V_{IN} \le –V_{REF}$, the output code is clamped at 0 (all zeroes).

The LTC2452 includes a proprietary system that can, typically, digitize each input 8LSB above V_{REF} and below GND, if the differential input is within $\pm V_{REF}$. As an example (Figure 3), if the user desires to measure a signal slightly below ground, the user could set $V_{IN}^–$ = GND, and V_{REF} = 5V. If V_{IN}^+ = GND, the output code would be approximately 32768. If V_{IN}^+ = GND – 8LSB = –1.22 mV, the output code would be approximately 32760.

The total amount of overrange and underrange capability is typically 31LSB for a given device. The 31LSB total is distributed between the overrange and underrange capability. For example, if the underrange capability is 8LSB, the overrange capability is typically 31 – 8 = 23LSB.

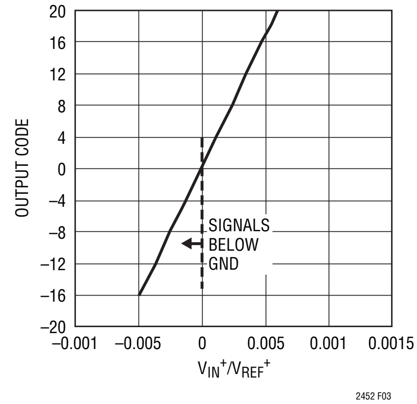

Figure 3. Output Code vs V_{IN}^+ with $V_{IN}^–$ = 0

Output Data Format

The LTC2452 generates a 16-bit direct binary encoded result. It is provided as a 16-bit serial stream through the SDO output pin under the control of the SCK input pin (see Figure 4).

Letting $V_{IN} = (V_{IN}^+ – V_{IN}^–)$, the output code is given as 32768 • V_{IN}/V_{REF} + 32768. The first bit output by the LTC2452, D15, is the MSB, which is 1 for $V_{IN}^+ \ge V_{IN}^–$ and 0 for $V_{IN}^+ < V_{IN}^–$. This bit is followed by successively less significant bits (D14, D13...) until the LSB is output by the LTC2452. Table 1 shows some example output codes.

During the data output operation the $\overline{CS}$ input pin must be pulled low ($\overline{CS}$ = LOW). The data output process starts

Table 1. LTC2452 Output Data Format

DIFFERENTIAL INPUT VOLTAGE $V_{IN}^+ – V_{IN}^–$	D15 (MSB)	D14	D13	D12…D2	D1	D0 (LSB)	CORRESPONDING DECIMAL VALUE
$\ge V_{REF}$	1	1	1	1	1	1	65535
V_{REF} – 1LSB	1	1	1	1	1	0	65534
0.5•V_{REF}	1	1	0	0	0	0	49152
0.5•V_{REF} – 1LSB	1	0	1	1	1	1	49151
0	1	0	0	0	0	0	32768
–1LSB	0	1	1	1	1	1	32767
–0.5•V_{REF}	0	1	0	0	0	0	16384
–0.5•V_{REF} – 1LSB	0	0	1	1	1	1	16383
$\le –V_{REF}$	0	0	0	0	0	0	0

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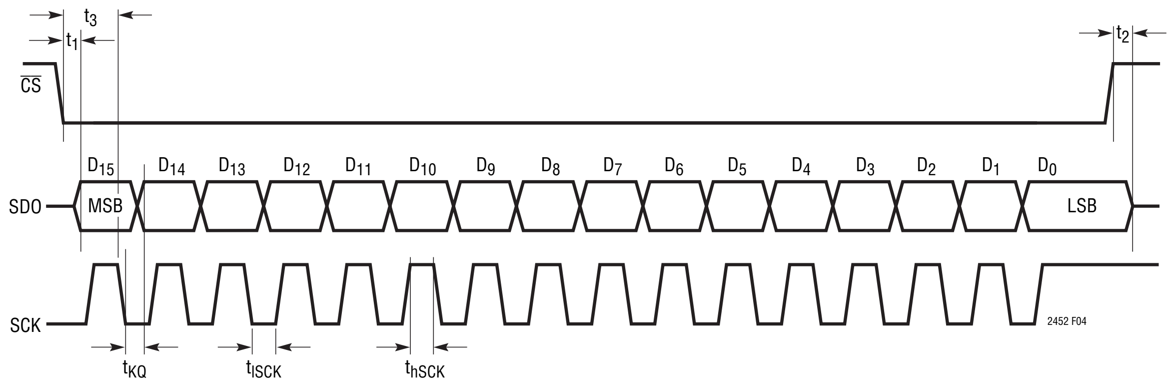

Figure 4. Data Output Timing

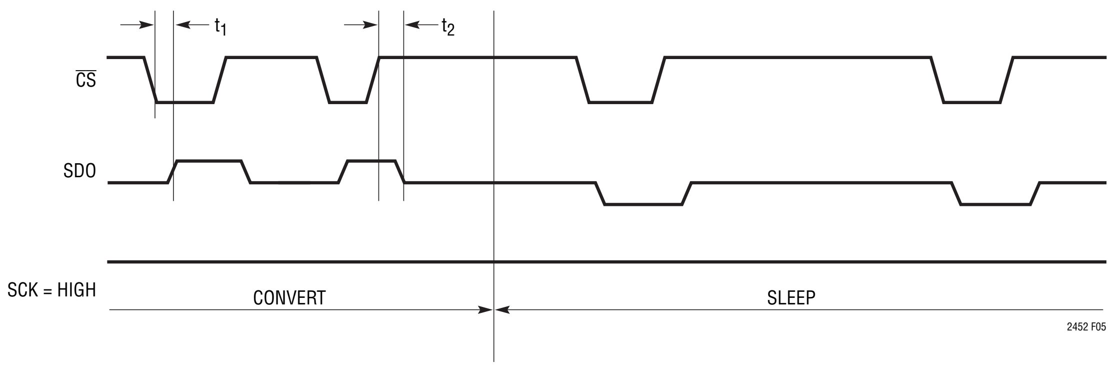

Figure 5. Conversion Status Monitoring Mode

with the most significant bit of the result being present at the SDO output pin (SDO = D15) once $\overline{CS}$ goes low. A new data bit appears at the SDO output pin after each falling edge detected at the SCK input pin. The output data can be reliably latched by the user using the rising edge of SCK.

Conversion Status Monitor

For certain applications, the user may wish to monitor the LTC2452 conversion status. This can be achieved by holding SCK HIGH during the conversion cycle. In this condition, whenever the $\overline{CS}$ input pin is pulled low ($\overline{CS}$ = LOW), the SDO output pin will provide an indication of the conversion status. SDO = HIGH is an indication of a conversion cycle in progress while SDO = LOW is an indication of a completed conversion cycle. An example of such a sequence is shown in Figure 5.

Conversion status monitoring, while possible, is not required for LTC2452 as its conversion time is fixed and equal at approximately 16.6ms (23ms maximum). Therefore, external timing can be used to determine the completion of a conversion cycle.

SERIAL INTERFACE

The LTC2452 transmits the conversion result and receives the start of conversion command through a synchronous 3-wire interface. This interface can be used during the CONVERT and SLEEP states to assess the conversion status and during the DATA OUTPUT state to read the conversion result, and to trigger a new conversion.

Serial Interface Operation Modes

The modes of operation can be summarized as follows:

1) The LTC2452 functions with SCK idle high (commonly known as CPOL = 1) or idle low (commonly known as CPOL = 0).

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2) After the 16th bit is read, the user can choose one of two ways to begin a new conversion. First, one can pull $\overline{CS}$ high ($\overline{CS}$ = ↑). Second, one can use a high-low transition on SCK (SCK = ↓).

3) At any time during the Data Output state, pulling $\overline{CS}$ high ($\overline{CS}$ = ↑) causes the part to leave the I/O state, abort the output and begin a new conversion.

4) When SCK = HIGH, it is possible to monitor the conversion status by pulling $\overline{CS}$ low and watching for SDO to go low. This feature is available only in the idle-high (CPOL = 1) mode.

Serial Clock Idle-High (CPOL = 1) Examples

In Figure 6, following a conversion cycle the LTC2452 automatically enters the low power sleep mode. The user can monitor the conversion status at convenient intervals using $\overline{CS}$ and SDO.

Pulling $\overline{CS}$ LOW while SCK is HIGH tests whether or not the chip is in the CONVERT state. While in the CONVERT state, SDO is HIGH while $\overline{CS}$ is LOW. In the SLEEP state, SDO is LOW while $\overline{CS}$ is LOW. These tests are not required operational steps but may be useful for some applications.

When the data is available, the user applies 16 clock cycles to transfer the result. The $\overline{CS}$ rising edge is then used to initiate a new conversion.

The operation example of Figure 7 is identical to that of Figure 6, except the new conversion cycle is triggered by the falling edge of the serial clock (SCK). A 17th clock pulse is used to trigger a new conversion cycle.

Serial Clock Idle-Low (CPOL = 0) Examples

In Figure 8, following a conversion cycle the LTC2452 automatically enters the low-power sleep state. The user determines data availability (and the end of conversion)

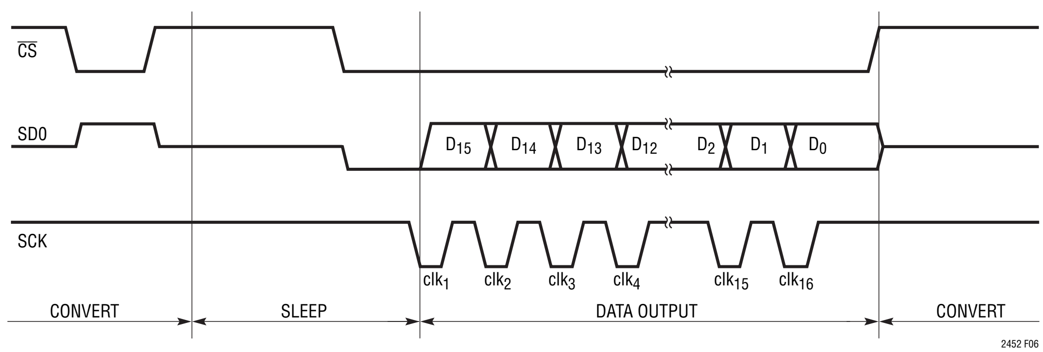

Figure 6. Idle-High (CPOL = 1) Serial Clock Operation Example. The Rising Edge of $\overline{CS}$ Starts a New Conversion

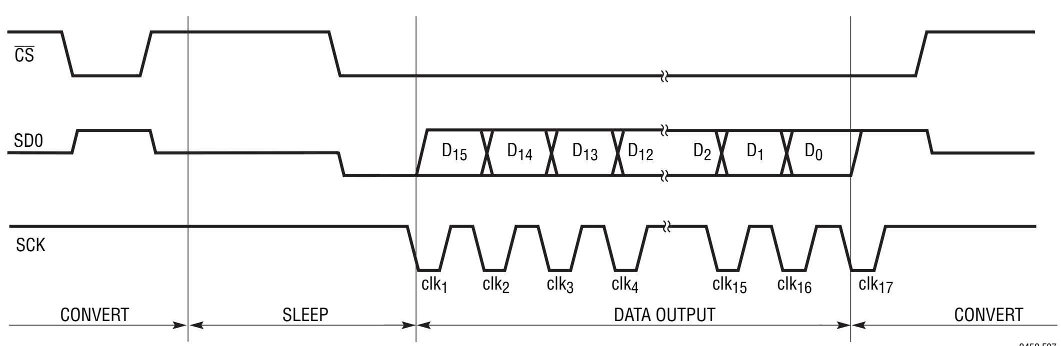

Figure 7. Idle-High (CPOL = 1) Clock Operation Example. A 17th Clock Pulse is Used to Trigger a New Conversion Cycle

APPLICATIONS INFORMATION

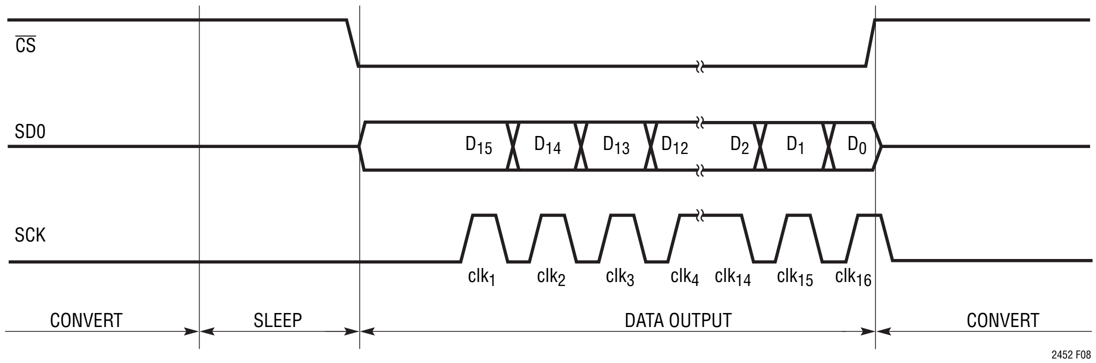

Figure 8. Idle-Low (CPOL = 0) Clock. $\overline{CS}$ Triggers a New Conversion

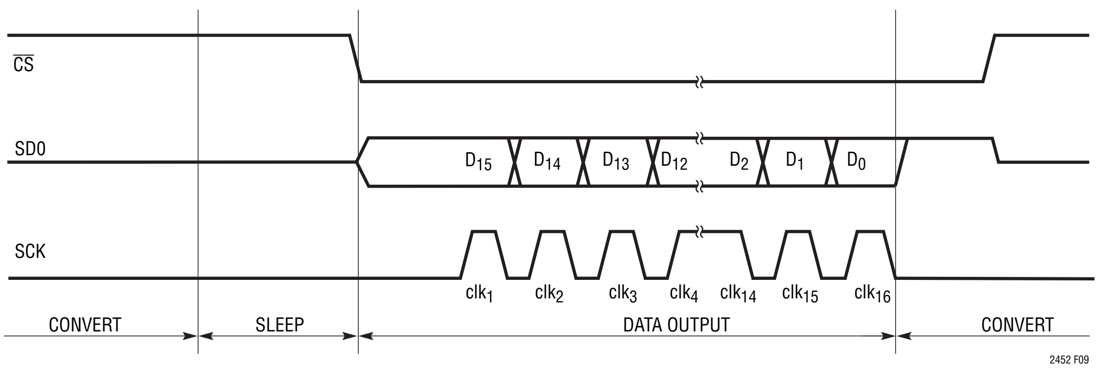

Figure 9. Idle-Low (CPOL = 0) Clock. The 16th SCK Falling Edge Triggers a New Conversion

based upon external timing. The user then pulls $\overline{CS}$ low ($\overline{CS}$ = ↓) and uses 16 clock cycles to transfer the result. Following the 16th rising edge of the clock, $\overline{CS}$ is pulled high ($\overline{CS}$ = ↑), which triggers a new conversion.

The timing diagram in Figure 9 is identical to that of Figure 8, except in this case a new conversion is triggered by SCK. The 16th SCK falling edge triggers a new conversion cycle and the $\overline{CS}$ signal is subsequently pulled high.

Examples of Aborting Cycle Using $\overline{CS}$

For some applications, the user may wish to abort the I/O cycle and begin a new conversion. If the LTC2452 is in the data output state, a $\overline{CS}$ rising edge clears the remaining data bits from the output registers, aborts the output cycle and triggers a new conversion. Figure 10 shows an example of aborting an I/O with idle-high (CPOL = 1) and Figure 11 shows an example of aborting an I/O with idle-low (CPOL = 0).

A new conversion cycle can be triggered using the $\overline{CS}$ signal without having to generate any serial clock pulses as shown in Figure 12. If SCK is maintained at a low logic level, after the end of a conversion cycle, a new conversion operation can be triggered by pulling $\overline{CS}$ low and then high. When $\overline{CS}$ is pulled low ($\overline{CS}$ = LOW), SDO will output the sign (D15) of the result of the just completed conversion. While a low logic level is maintained at SCK

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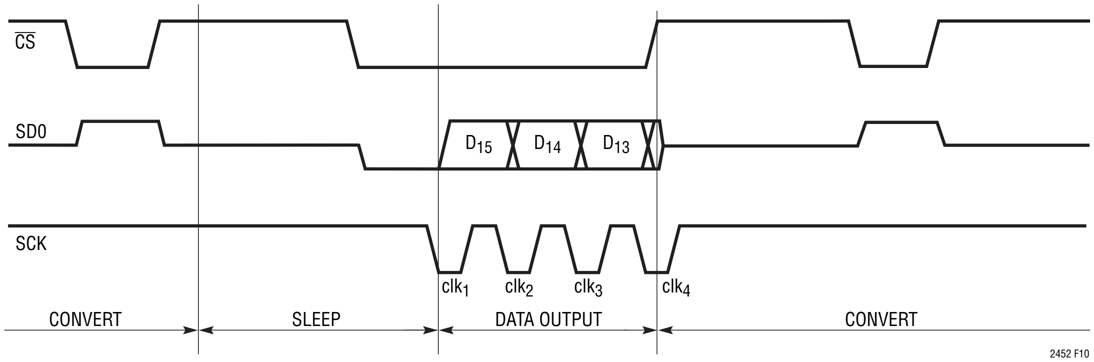

Figure 10. Idle-High (CPOL = 1) Clock and Aborted I/O Example

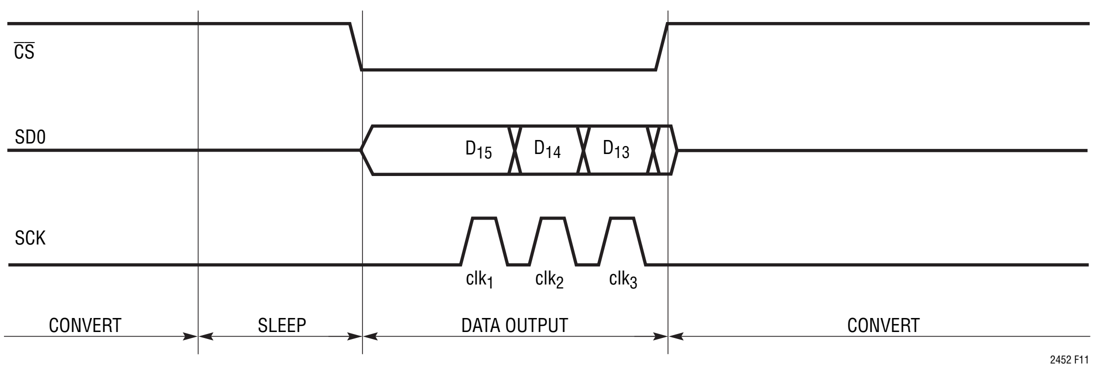

Figure 11. Idle-Low (CPOL = 0) Clock and Aborted I/O Example

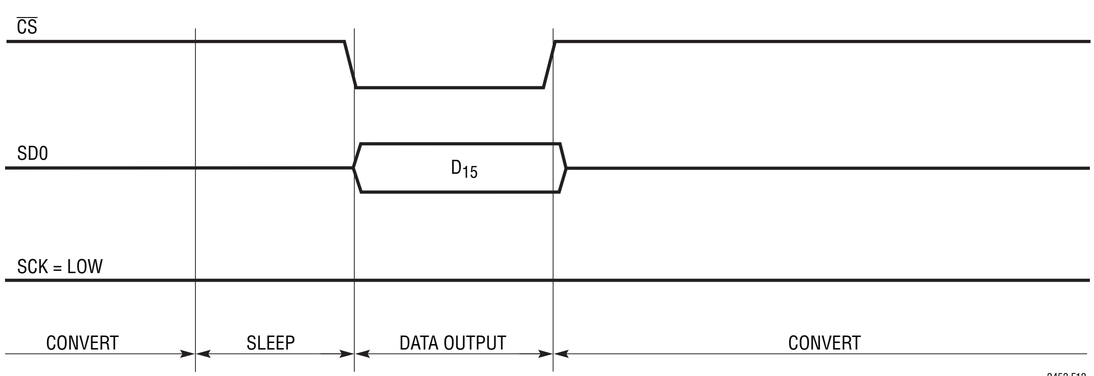

Figure 12. Idle-Low (CPOL = 0) Clock and Minimum Data Output Length Example

APPLICATIONS INFORMATION

pin and $\overline{CS}$ is subsequently pulled high ($\overline{CS}$ = HIGH) the remaining 15 bits of the result (D14:D0) are discarded and a new conversion cycle starts.

Following the aborted I/O, additional clock pulses in the CONVERT state are acceptable, but excessive signal transitions on SCK can potentially create noise on the ADC during the conversion, and thus may negatively influence the conversion accuracy.

2-Wire Operation

The 2-wire operation modes, while reducing the number of required control signals, should be used only if the LTC2452 low power sleep capability is not required. In addition the option to abort serial data transfers is no longer available. Hardwire $\overline{CS}$ to GND for 2-wire operation.

Figure 13 shows a 2-wire operation sequence which uses an idle-high (CPOL = 1) serial clock signal. The conversion status can be monitored at the SDO output. Following a conversion cycle, the ADC enters SLEEP state and the SDO output transitions from HIGH to LOW. Subsequently 16 clock pulses are applied to the SCK input in order to serially shift the 16 bit result. Finally, the 17th clock pulse is applied to the SCK input in order to trigger a new conversion cycle.

Figure 14 shows a 2-wire operation sequence which uses an idle-low (CPOL = 0) serial clock signal. The conversion status cannot be monitored at the SDO output. Following a conversion cycle, the LTC2452 bypasses the SLEEP state and immediately enters the DATA OUTPUT state. At this moment the SDO pin outputs the sign (D15) of the conversion result. The user must use external timing in order to determine the end of conversion and result availability. Subsequently 16 clock pulses are applied to SCK in order to serially shift the 16-bit result. The 16th clock falling edge triggers a new conversion cycle.

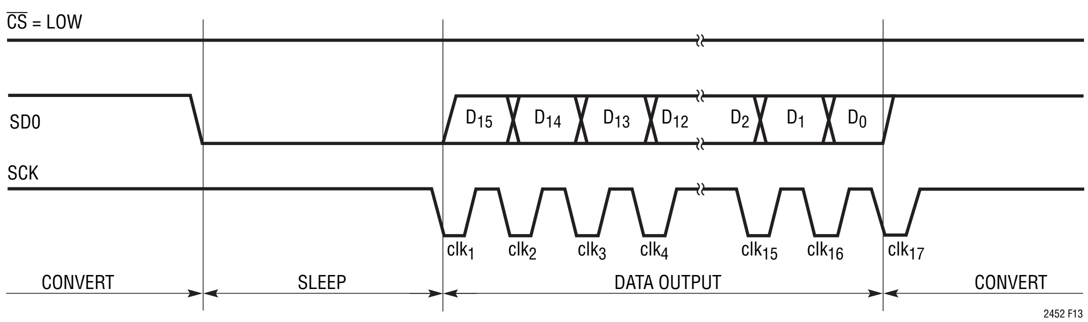

Figure 13. 2-Wire, Idle-High (CPOL = 1) Serial Clock, Operation Example

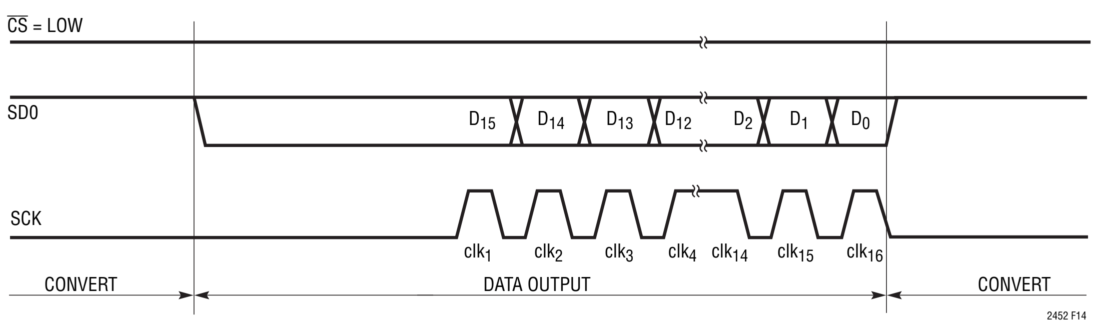

Figure 14. 2-Wire, Idle-Low (CPOL = 0) Serial Clock Operation Example

APPLICATIONS INFORMATION

PRESERVING THE CONVERTER ACCURACY

The LTC2452 is designed to minimize the conversion result's sensitivity to device decoupling, PCB layout, anti-aliasing circuits, line and frequency perturbations. Nevertheless, in order to preserve the high accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

Due to the nature of CMOS logic, it is advisable to keep input digital signals near GND or V_{CC}. Voltages in the range of 0.5V to V_{CC} – 0.5V may result in additional current leakage from the part. Undershoot and overshoot should also be minimized, particularly while the chip is converting. It is thus beneficial to keep edge rates of about 10ns and limit overshoot and undershoot to less than 0.3V.

Noisy external circuitry can potentially impact the output under 2-wire operation. In particular, it is possible to get the LTC2452 into an unknown state if an SCK pulse is missed or noise triggers an extra SCK pulse. In this situation, it is impossible to distinguish SDO = 1 (indicating conversion in progress) from valid "1" data bits. As such, CPOL = 1 is recommended for the 2-wire mode. The user should look for SDO = 0 before reading data, and look for SDO = 1 after reading data. If SDO does not return a "0" within the maximum conversion time (or return a "1" after a full data read), generate 16 SCK pulses to force a new conversion.

Driving V_{CC} and GND

In relation to the V_{CC} and GND pins, the LTC2452 combines internal high frequency decoupling with damping elements, which reduce the ADC performance sensitivity to PCB layout and external components. Nevertheless, the very high accuracy of this converter is best preserved by careful low and high frequency power supply decoupling.

A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF ceramic capacitor should be connected between the V_{CC} and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC package. It is also desirable to avoid any via in the circuit path, starting from the converter V_{CC} pin, passing through these two decoupling capacitors, and returning to the converter GND pin. The area encompassed by this circuit path, as well as the path length, should be minimized.

Furthermore, as shown in Figure 15, GND is used as the negative reference voltage. It is thus important to keep the GND line quiet and connect GND through a low-impedance trace.

Very low impedance ground and power planes, and star connections at both V_{CC} and GND pins, are preferable. The V_{CC} pin should have two distinct connections: the first to the decoupling capacitors described above, and the second to the ground return for the power supply voltage source.

Driving REF

A simplified equivalent circuit for REF is shown in Figure 15. Like all other A/D converters, the LTC2452 is only as accurate as the reference it is using. Therefore, it is important to keep the reference line quiet by careful low and high frequency decoupling.

The LT6660 reference is an ideal match for driving the LTC2452's REF pin. The LTC6660 is available in a 2mm × 2mm DFN package with 2.5V, 3V, 3.3V and 5V options.

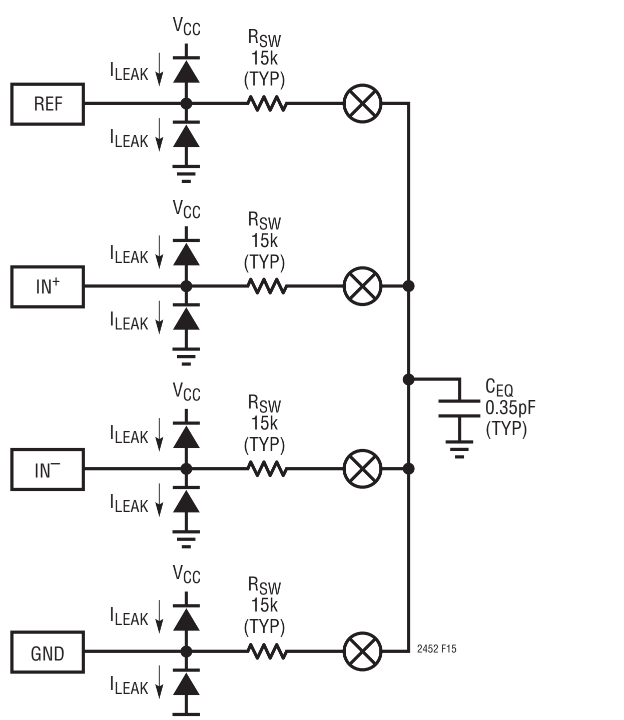

Figure 15. LTC2452 Analog Input/Reference Equivalent Circuit

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A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF ceramic capacitor should be connected between the REF and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC.

Driving V_{IN}^+ and V_{IN}^-

The input drive requirements can best be analyzed using the equivalent circuit of Figure 16. The input signal V_{SIG} is connected to the ADC input pins (IN^+ and IN^-) through an equivalent source resistance R_S. This resistor includes both the actual generator source resistance and any additional optional resistors connected to the input pins. Optional input capacitors C_{IN} are also connected to the ADC input pins. This capacitor is placed in parallel with the ADC input parasitic capacitance C_{PAR}. Depending on the PCB layout, C_{PAR} has typical values between 2pF and 15pF. In addition, the equivalent circuit of Figure 16 includes the converter equivalent internal resistor R_{SW} and sampling capacitor C_{EQ}.

There are some immediate trade-offs in R_S and C_{IN} without needing a full circuit analysis. Increasing R_S and C_{IN} can give the following benefits:

1) Due to the LTC2452's input sampling algorithm, the input current drawn by either V_{IN}^+ or V_{IN}^- over a conversion cycle is typically 50nA. A high $R_S \bullet C_{IN}$ attenuates the high frequency components of the input current, and R_S values up to 1k result in <1LSB error.

2) The bandwidth from V_{SIG} is reduced at the input pins (IN^+, IN^-). This bandwidth reduction isolates the ADC from high frequency signals, and as such provides simple anti-aliasing and input noise reduction.

3) Switching transients generated by the ADC are attenuated before they go back to the signal source.

4) A large C_{IN} gives a better AC ground at the input pins, helping reduce reflections back to the signal source.

5) Increasing R_S protects the ADC by limiting the current during an outside-the-rails fault condition.

There is a limit to how large $R_S \bullet C_{IN}$ should be for a given application. Increasing R_S beyond a given point increases the voltage drop across R_S due to the input current, to the point that significant measurement errors exist. Additionally, for some applications, increasing the $R_S \bullet C_{IN}$ product too much may unacceptably attenuate the signal at frequencies of interest.

For most applications, it is desirable to implement C_{IN} as a high-quality 0.1µF ceramic capacitor and $R_S \le 1k$. This capacitor should be located as close as possible to the actual V_{IN} package pin. Furthermore, the area encompassed by this circuit path, as well as the path length, should be minimized.

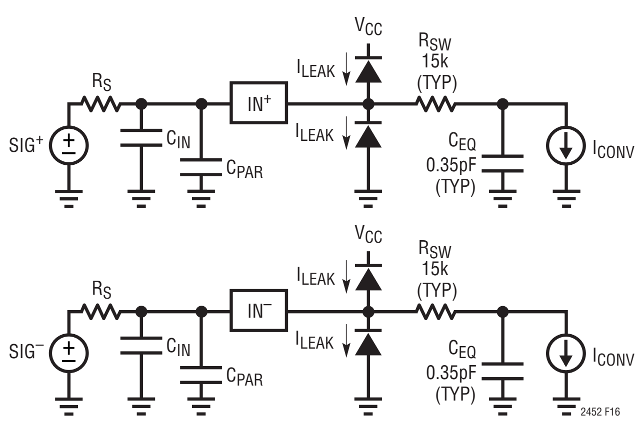

Figure 16. LTC2452 Input Drive Equivalent Circuit

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In the case of a 2-wire sensor that is not remotely grounded, it is desirable to split R_S and place series resistors in the ADC input line as well as in the sensor ground return line, which should be tied to the ADC GND pin using a star connection topology.

Figure 17 shows the measured LTC2452 INL vs Input Voltage as a function of R_S value with an input capacitor C_{IN} = 0.1µF.

In some cases, R_S can be increased above these guidelines. The input current is zero when the ADC is either in sleep or I/O modes. Thus, if the time constant of the input RC circuit $\tau = R_S \bullet C_{IN}$, is of the same order of magnitude or longer than the time periods between actual conversions, then one can consider the input current to be reduced correspondingly.

These considerations need to be balanced out by the input signal bandwidth. The 3dB bandwidth $\approx 1/(2\pi R_S C_{IN})$.

Finally, if the recommended choice for C_{IN} is unacceptable for the user's specific application, an alternate strategy is to eliminate C_{IN} and minimize C_{PAR} and R_S. In practical terms, this configuration corresponds to a low impedance sensor directly connected to the ADC through minimum length traces. Actual applications include current measurements through low value sense resistors, temperature measurements, low impedance voltage source monitoring, and so on. The resultant INL vs V_{IN} is shown in Figure 18. The measurements of Figure 18 include a capacitor C_{PAR} corresponding to a minimum sized layout pad and a minimum width input trace of about 1 inch length.

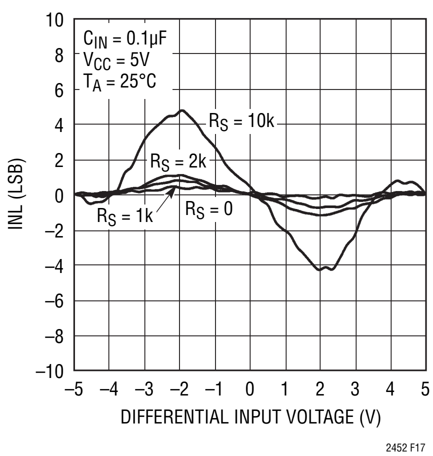

Figure 17. Measured INL vs Input Voltage, C_{IN} = 0.1µF, V_{CC} = 5V, T_A = 25°C

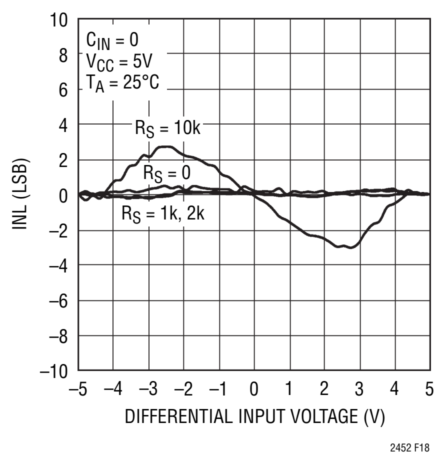

Figure 18. Measured INL vs Input Voltage, C_{IN} = 0, V_{CC} = 5V, T_A = 25°C

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Signal Bandwidth, Transition Noise and Noise Equivalent Input Bandwidth

The LTC2452 includes a SINC[1] type digital filter with the first notch located at f_0 = 60Hz. As such, the 3dB input signal bandwidth is 26.54Hz. The calculated LTC2452 input signal attenuation vs frequency over a wide frequency range is shown in Figure 19. The calculated LTC2452 input signal attenuation vs frequency at low frequencies is shown in Figure 20. The converter noise level is about 2.2µV_{RMS} and can be modeled by a white noise source connected at the input of a noise-free converter.

On a related note, the LTC2452 uses two separate A/D converters to digitize the positive and negative inputs. Each of these A/D converters has 2.2µV_{RMS} transition noise. If one of the input voltages is within this small transition noise band, then the output will fluctuate one bit, regardless of the value of the other input voltage. If both of the input voltages are within their transition noise bands, the output can fluctuate 2 bits.

For a simple system noise analysis, the V_{IN} drive circuit can be modeled as a single-pole equivalent circuit characterized by a pole location f_i and a noise spectral density n_i. If the converter has an unlimited bandwidth, or at least a bandwidth substantially larger than f_i, then the total noise contribution of the external drive circuit would be:

$$V_n = n_i \sqrt{\pi / 2 \bullet f_i}$$

Then, the total system noise level can be estimated as the square root of the sum of (V_n^2) and the square of the LTC2452 noise floor (~2.2µV^2).

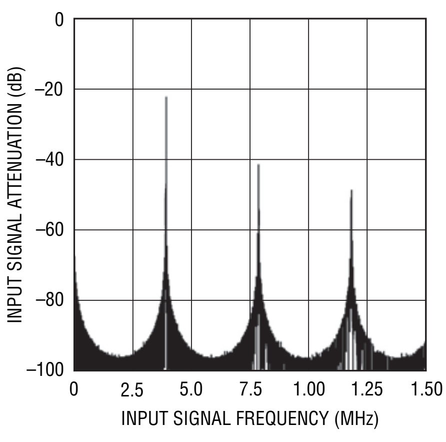


Figure 19. LTC2452 Input Signal Attenuation vs Frequency

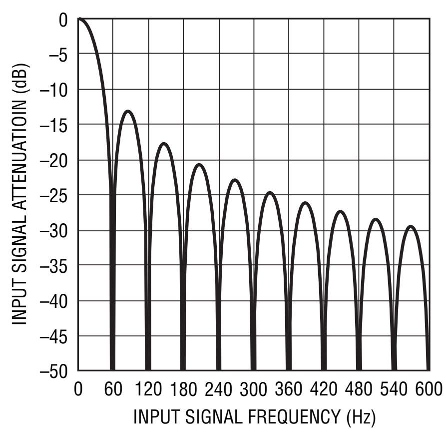
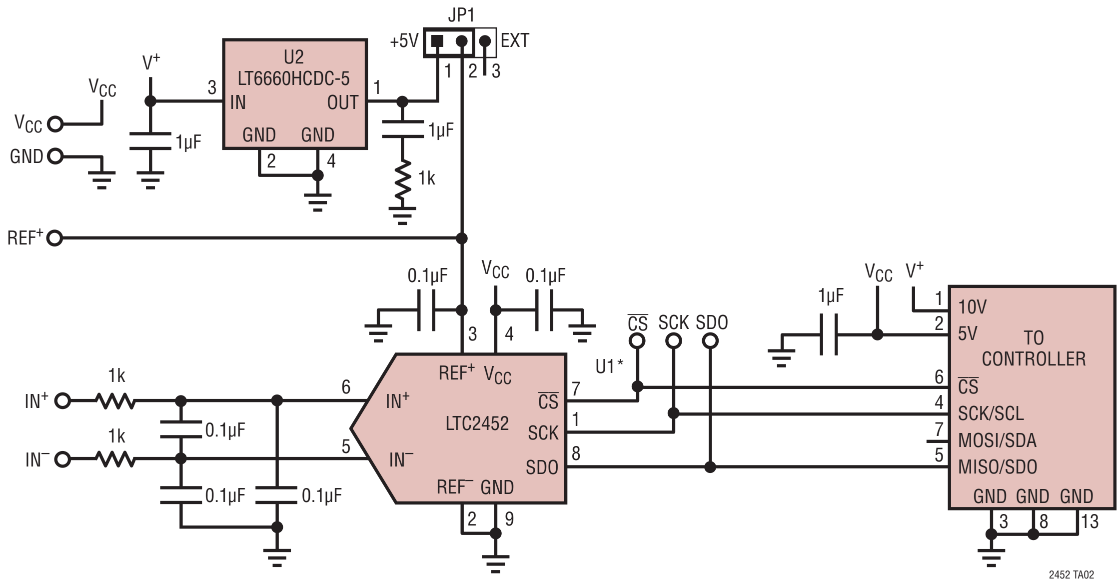


Figure 20. LTC2452 Input Signal Attenuation vs Frequency (Low Frequencies)

TYPICAL APPLICATION

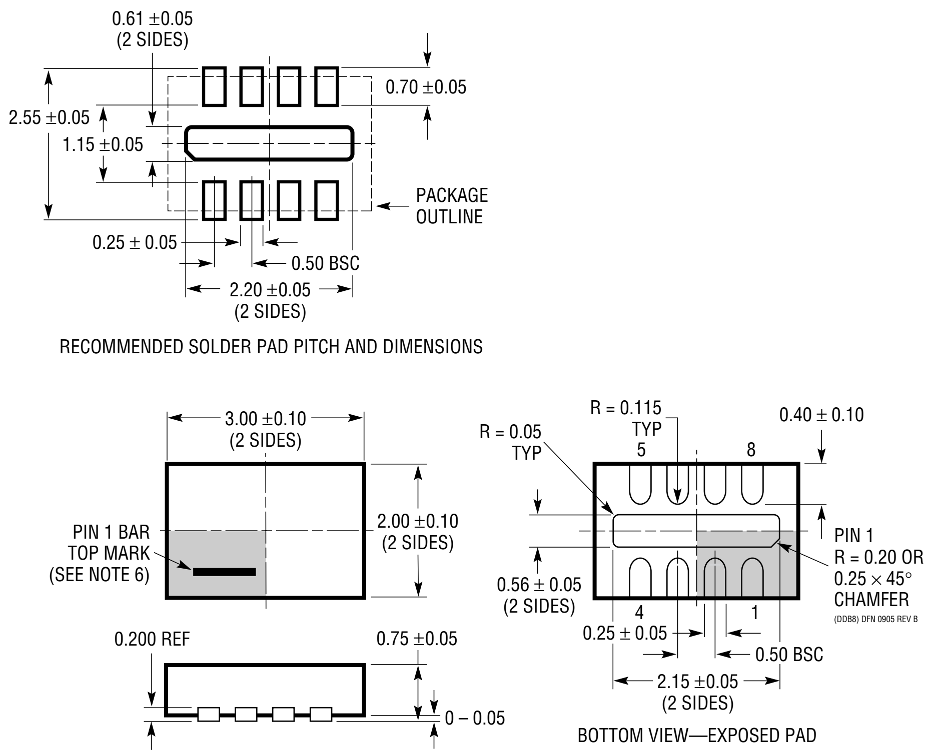


2452fd

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)

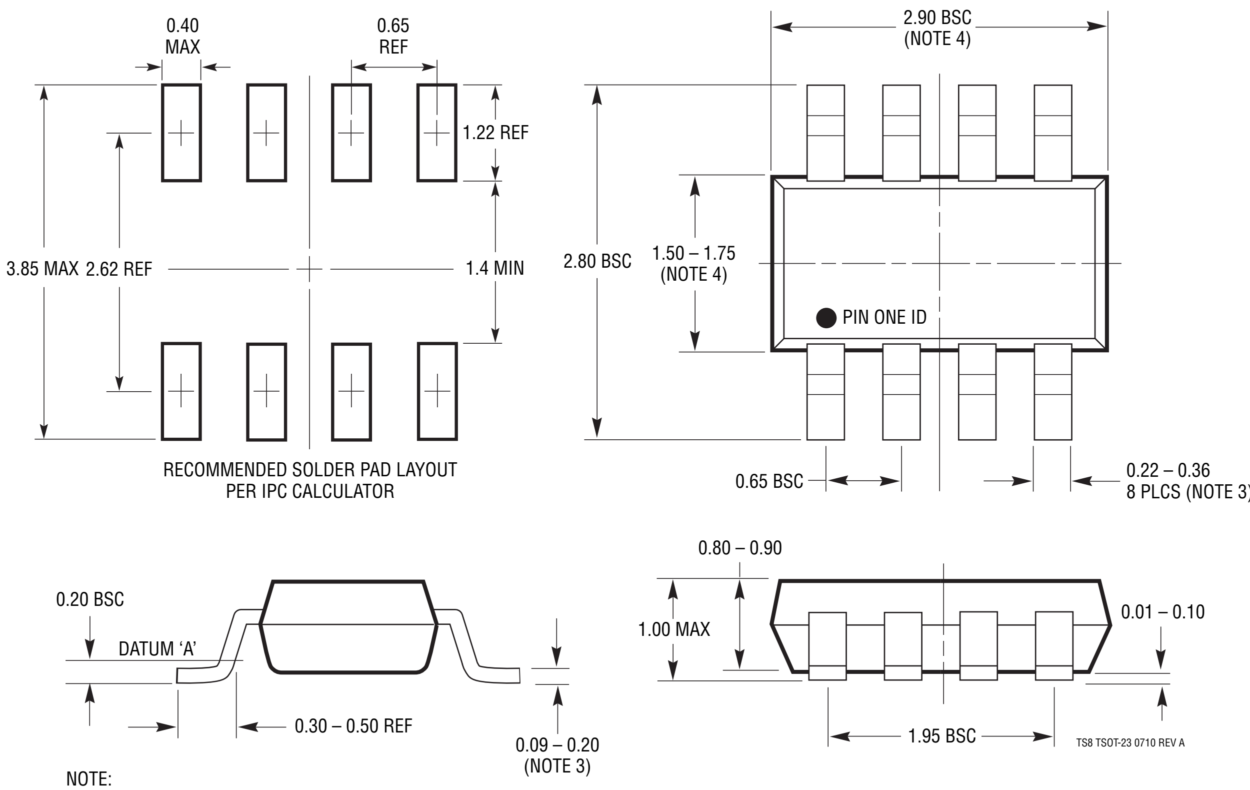


NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	03/10	Updated Analog Inputs and References section	3
		Added text to Input Voltage Range section	8
D	03/14	Changed V_{IN}^+ and V_{IN}^- Input Voltage Range (MAX) to V_{REF}	3

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1461	Micropower Series Reference, 2.5V	0.04% Max, 3ppm/°C Drift
LT1790	Micropower Precision Reference in TSOT-23-6 Package	60µA Max Supply Current, 10ppm/°C Max Drift, 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V Options
LTC2440	24-Bit No Latency ΔΣ™ ADC	200nV$_{RMS}$ Noise, 4kHz Output Rate, 15ppm INL
LTC2480	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temp. Sensor, SPI	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2481	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temp. Sensor, I^{2}C	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2482	16-Bit, Differential Input, No Latency ΔΣ ADC, SPI	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2483	16-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2484	24-Bit, Differential Input, No Latency ΔΣ ADC, SPI with Temp. Sensor	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2485	24-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C with Temp. Sensor	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC6241	Dual, 18MHz, Low Noise, Rail-to-Rail Op Amp	550nV$_{P-P}$ Noise, 125µV Offset Max
LT6660	Micropower References in 2mm × 2mm DFN Package, 2.5V, 3V, 3.3V, 5V	20ppm/°C Max Drift, 0.2% Max
LTC2450/LTC2450-1	Easy-to-Use, Ultra-Tiny 16-Bit ADC, SPI	2 LSB INL, 50nA Sleep Current, Tiny 2mm × 2mm DFN-6 Package, 30Hz/60Hz Output Rate
LTC2451/LTC2453	Easy-to-Use, Ultra-Tiny 16-Bit Single-Ended/Differential ADC, I^{2}C	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package, Programmable 30Hz/60Hz Output Rates
LTC2470/LTC2472	Selectable 233sps/833sps, 16-Bit ADC, SPI, Single-Ended/ Differential	10ppm/°C Integrated Precision Reference, 3mm × 3mm DFN-12 or MSOP-12 Package
LTC2471/LTC2473	Selectable 233sps/833sps, 16-Bit Single-Ended/Differential ADC, I^{2}C	10ppm/°C Integrated Precision Reference, 3mm × 3mm DFN-12 or MSOP-12 Package

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