PRODUCT CHANGE NOTIFICATION

LT LINEAR TECHNOLOGY

Linear Technology Corporation
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August 16, 2016   PCN#081616

Dear Sir/Madam:

Subject: <u>Notification of Change to LTC3887/LTC3887-1 Die and Datasheet</u>

Please be advised that Linear Technology Corporation has made enhancements to the LTC3887/LTC3887-1 product die to improve performance in the following areas:

1) Fix errata
2) Reduce power up times
3) Reduced TON_MIN
4) Reduce the ADC update period
5) Support I^{2}C PMBus thresholds compatible with bus power supplies as low as 1.8 volts
6) Improve on-chip EEPROM robustness

The documented errata in the LTC3887 are eliminated. Refer to the following link for the current errata documents http://cds.linear.com/docs/en/spec-notice/er3887f.pdf.

T$_{INIT}$, the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 70ms to 30ms for the LTC3887/LTC3887-1. This may allow applications to power up faster after application of VIN. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner.

TON_MIN will be reduced from nominally 90ns to 45ns to support large step down ratios at relatively high switching frequencies. The ADC update period, T$_{CONVERT}$, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters.

I^{2}C thresholds are reduced to support PMBus communication with other ICs using I/O interface supplies as low as 1.8 volts. The V$_{IL}$ and V$_{IH}$ specifications for the SDA, SCL, RUN0, RUN1, GPIO0 and GPIO1 pins are reduced from 1.4V and 2.0V, respectively, to 0.8V and 1.35V. The LTC3887/LTC3887-1 is fully compliant with PMBus 1.2. For more details, please refer to PMBus 1.2 revisions on the PMBus website http://pmbus.org/Specifications/OlderSpecifications and the SMBus Specification Version 2.0 at http://smbus.org/specs/smbus20.pdf.

The above changes are shown on the attached pages of the marked up datasheet.
Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming

files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth events are a repeat of the fourth event if the part is reset. However, when reading the fault log from RAM, all 6 events of cyclical data are available.

The new silicon can be identified with the MFR_SPECIAL_ID, PMBus command code 0xE7, with a value of 0x470* where * is a value of 8-F.

The only change to the PWM characteristics of the LTC3887/LTC3887-1 is the reduction in TON_MIN. The die changes were qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. The revised product will have successfully completed 1000 hours burn-in before production release. Product built using the new dice will be available for shipment with an approximate datecode of 1713.

Should you have any further questions, please feel free to contact your local Linear Technology sales person or you may contact me at 408-432-1900 ext. 2374, or by E-mail DJANI@LINEAR.COM. If I do not hear from you by October 17, 2016, we will consider this change approved by your company.

Sincerely,

Daksha Jani
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range	(Note 12)	●	4.5		24	V
I_Q	Input Voltage Supply Current Normal Operation	$V_{RUN0,1}$ = 3.3V, No Caps on TG and BG			25		mA
		$V_{RUN0,1}$ = 0V			20		mA
V_{UVLO}	Undervoltage Lockout Threshold when V_{IN} > 4.3V	V_{INTVCC} Falling			3.7		V
		V_{INTVCC} Rising			3.95		V
T_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts.		~~70~~ 30			ms
Control Loop							
V_{OUTR0}	Full-Scale Voltage High Range	VOUT_COMMAND = 5.500V (Note 9)	●	5.45		5.55	V
	Set Point Accuracy (0.6V to 5V)		●	–0.5		0.5	%
	Resolution				12		Bits
	LSB Step Size				1.375		mV
V_{OUTR1}	Full-Scale Voltage Low Range	VOUT_COMMAND = 2.75V (Note 9)	●	2.7		2.8	V
	Set Point Accuracy (0.6V to 2.5V)		●	–0.5		0.5	%
	Resolution				12		Bits
	LSB Step Size				0.6875		mV
$V_{LINEREG}$	Line Regulation	6V < V_{IN} < 24V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V – 0.7V	●		0.01	0.1	%
		ΔV_{ITH} = 1.35V – 2.0V	●		–0.01	–0.1	%
$g_{m0,1}$	Error Amplifier g_m	$I_{TH0,1}$ =1.22V			3		mmho
$I_{ISENSE0,1}$	Input Current	V_{ISENSE} = 5.5V	●		±1	±3	µA
$V_{SENSERIN0}$	V_{SENSE} Input Resistance to Ground	0V ≤ V_{PIN} ≤ 5.5V			41		kΩ
$V_{SENSERIN1}$	V_{SENSE} Input Resistance to Ground	0V ≤ V_{PIN} ≤ 5.5V			37		kΩ
$V_{IILIMIT}$	Resolution				3		bits
	$V_{ILIMMAX}$	Hi Range	●	68	75	82	mV
		Lo Range	●	44	50	56	mV
	V_{ILMMIN}	Hi Range			37.5		mV
		Lo Range			25		mV
Gate Drivers LTC3887							
TG0,1 t_r t_f	TG Transition Time (LTC3887/LTC3887-1) Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			30 30		ns ns
BG0,1 t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			30 30		ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time (LTC3887/LTC3887-1)			~~90~~ 45			ns
OV Output Voltage Supervisor							
N	Resolution				8		Bits
V_{RANGE0}	Voltage Monitoring Range	Range Value = 0		1		5.6	V
V_{RANGE1}	Voltage Monitoring Range	Range Value = 1		0.5		2.7	V
V_{OUSTP0}	Threshold Programming Step	Range Value = 0			22.5		mV
V_{OUSTP1}	Threshold Programming Step	Range Value = 1			11.25		mV
V_{THACC0}	Threshold Accuracy 2V < V_{OUT} < 5V	Range Value = 0	●			±2	%
V_{THACC1}	Threshold Accuracy 1V < V_{OUT} < 2.5V	Range Value = 1	●			±2	%
t_{PROPOV}	OV Comparator to GPIO Low Time	V_{OD} = 10% of Threshold				35	µs

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
UV Output Voltage Supervisor							
N	Resolution				8		bits
V_{RANGE0}	Voltage Range	High Range		1		5.5	V
V_{RANGE1}	Voltage Range	Low Range		0.5		2.7	V
V_{OUSTP0}	Step Size	Range Value = 0, High Range			22		mV
V_{OUSTP1}	Step Size	Range Value = 1, Low Range			11		mV
V_{THACC0}	Threshold Accuracy 2V < V_{OUT} < 5V	Range Value = 0, High Range	●			±2	%
V_{THACC1}	Threshold Accuracy 1V < V_{OUT} < 2.5V	Range Value = 1, Low Range	●			±2	%
t_{PROPUV}	UV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				100	μs
V_{IN} Voltage Supervisor							
N	Resolution				8		bits
$V_{INRANGE}$	Full-Scale Voltage			4.5		20	V
V_{INSTP}	Step Size				82		mV
$V_{INTHACC}$	Threshold Accuracy 9.0V < V_{IN} < 20V		●			±2.5	%
$V_{INTHACCM}$	Threshold Accuracy 4.5V < V_{IN} ≤ 9V		●			±5	%
$t_{PROPVIN}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of Threshold				100	μs
Output Voltage Readback							
N	Resolution				16		Bits
	LSB Step Size				244		μV
V_{OFS}	Full-Scale Voltage	(Note 10) V_{RUNn} = 0V (Note 8)			8		V
V_{OUT_TUE}	Total Unadjusted Error	(Note 8) V_{OUTn} > 0.6V	●			0.5	%
V_{OS}	Zero-Code Offset Voltage				±500		μV
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
V_{IFS}	Full-Scale Voltage	(Note 11)			38.91		V
V_{IN_TUE}	Total Unadjusted Error	V_{VIN} > 4.5V (Note 8)				0.5	%
			●			2	%
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
Output Current Readback							
N	Resolution	(Note 5)			10		Bits
	LSB Step Size	$0V ≤ |V_{ISENSE}^+ - V_{ISENSE}^-| < 16mV$			15.625		μV
		$16mV ≤ |V_{ISENSE}^+ - V_{ISENSE}^-| < 32mV$			31.25		μV
		$32mV ≤ |V_{ISENSE}^+ - V_{ISENSE}^-| < 63.9mV$			62.5		μV
		$63.9mV ≤ |V_{ISENSE}^+ - V_{ISENSE}^-| < 127.9mV$			125		μV
I_{FS}	Full-Scale Current	(Note 7) $R_{ISENSE} = 1m\Omega$			±128		A
I_{OUT_TUE}	Total Unadjusted Error	(Note 8) V_{ISENSE} > 6mV	●			±1	%
V_{OS}	Zero-Code Offset Voltage				±28		μV
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
Input Current and Duty Cycle Readback							
D_RES	Resolution				10		Bits
D_TUE	Total Unadjusted Error	16.3% Duty Cycle		–3		3	%
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~ 90		ms
Temperature Readback (T0, T1, T2)							
T_{RES_T}	Resolution				0.25		°C
T0,1_TUE	External TSNS TUE	ΔV_{TSNS} = 72mV (Note 8)	●			±3	°C
T2_TUE	Internal TSNS TUE	$V_{RUN0,1}$ = 0.0V, f_{SYNC} = 0kHz (Note 8)			±1		°C
$t_{CONVERT\_T}$	Update Rate	(Note 6)			~~100~~ 90		ms

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ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INTV$_{CC}$ Regulator							
V$_{INTVCC}$	Internal V$_{CC}$ Voltage No Load	6V < V$_{IN}$ < 24V		4.8	5	5.2	V
V$_{LDO\_INT}$	INTV$_{CC}$ Load Regulation	I$_{CC}$ = 0mA to 50mA			0.5	±2	%
V$_{DD33}$ Regulator							
V$_{DD33}$	Internal V$_{DD33}$ Voltage	4.5V < V$_{INTVCC}$		3.2	3.3	3.4	V
I$_{LIM(VDD33)}$	V$_{DD33}$ Current Limit	V$_{DD33}$ = GND			70		mA
V$_{DD33\_OV}$	V$_{DD33}$ Overvoltage Threshold				3.5		V
V$_{DD33\_UV}$	V$_{DD33}$ Undervoltage Threshold				3.1		V
V$_{DD25}$ Regulator							
V$_{DD25}$	Internal V$_{DD25}$ Voltage				2.5		V
I$_{LIM(VDD25)}$	V$_{DD25}$ Current Limit	V$_{DD25}$ = GND			50		mA
Oscillator and Phase-Locked Loop							
f$_{OSC}$	Oscillator Frequency Accuracy	250kHz < f$_{SYNC}$ < 1MHz Measured Falling Edge-to-Falling Edge of SYNC with SWITCH_FREQUENCY = 250.0 and 1000.0	●			±7.5	%
V$_{TH,SYNC}$	SYNC Input Threshold	V$_{CLKIN}$ Falling V$_{CLKIN}$ Rising			1 1.5		V V
V$_{OL,SYNC}$	SYNC Low Output Voltage	I$_{LOAD}$ = 3mA			0.2	0.4	V
I$_{LEAKSYNC}$	SYNC Leakage Current in Slave Mode	0V ≤ V$_{PIN}$ ≤ 3.6V				±5	µA
θSYNC-θ0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG_LTC3887[2:0] = 0, 2, 3 MFR_PWM_CONFIG_LTC3887[2:0] = 5 MFR_PWM_CONFIG_LTC3887[2:0] = 1 MFR_PWM_CONFIG_LTC3887[2:0] = 4, 6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG_LTC3887[2:0] = 3 MFR_PWM_CONFIG_LTC3887[2:0] = 0 MFR_PWM_CONFIG_LTC3887[2:0] = 2, 4, 5 MFR_PWM_CONFIG_LTC3887[2:0] = 1 MFR_PWM_CONFIG_LTC3887[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 13)	0°C < T$_J$ < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 13)	T$_J$ < T$_{JMAX}$	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < TJ < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, RUN0, RUN1, GPIO0, GPIO1							
V$_{IH}$	Input High Threshold Voltage	SCL, SDA, RUN0, RUN1, GPIO0, GPIO1	●			~~2.0~~ 1.35	V
V$_{IL}$	Input Low Threshold Voltage	SCL, SDA, RUN0, RUN1, GPIO0, GPIO1	●	~~1.4~~ 0.8			V
V$_{HYST}$	Input Hysteresis	SCL, SDA			0.08		V
C$_{PIN}$	Input Capacitance					10	pF
Digital Input WP							
I$_{PUWP}$	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, GPIO0, GPIO1, ALERT, RUN0, RUN1, SHARE_CLK							
V$_{OL}$	Output Low Voltage	I$_{SINK}$ = 3mA	●			0.4	V
Digital Inputs SHARE_CLK, WP							
V$_{IH}$	Input High Threshold Voltage				1.5	1.8	V
V$_{IL}$	Input Low Threshold Voltage			0.6	1		V
Leakage Current SDA, SCL, ALERT, RUN0, RUN1							
I$_{OL}$	Input Leakage Current	0V ≤ V$_{PIN}$ ≤ 5.5V	●			±5	µA