

# NCV891330

## Step-Down Regulator - Automotive, Low-Iq, Dual-Mode

**3 A, 2 MHz**

The NCV891330 is a Dual Mode regulator intended for Automotive, battery-connected applications that must operate with up to a 45 V input supply. Depending on the output load, it operates either as a PWM Buck Converter or as a Low Drop-Out Linear Regulator, and is suitable for systems with low noise and Low Quiescent Current requirements often encountered in automotive driver information systems. A reset pin (with fixed delay) simplifies interfacing with a microcontroller.

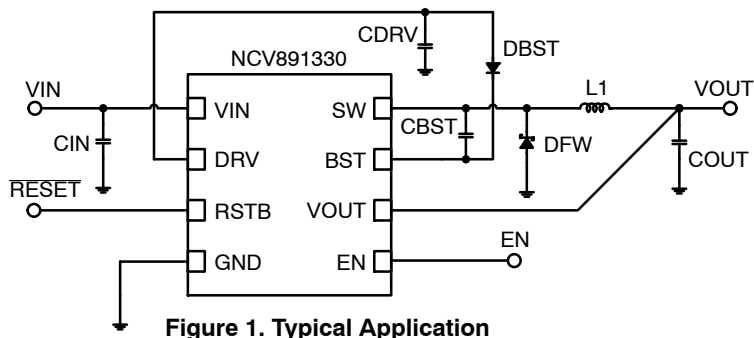
The NCV891330 also provides several protection features expected in automotive power supply systems such as current limit, short circuit protection, and thermal shutdown. In addition, the high switching frequency produces low output voltage ripple even when using small inductor values and an all-ceramic output filter capacitor – forming a space-efficient switching regulator solution.

### Features

- 30  $\mu$ A Iq in Light Load Condition
- 3.0 A Maximum Output Current in PWM Mode
- Internal N-channel Power Switch
- V<sub>IN</sub> Operating Range 3.7 V to 36 V
- Withstands Load Dump to 45 V
- Logic Level Enable Pin can be Tied to Battery
- Fixed Output Voltage of 5.0 V, 4.0 V, 3.8 V or 3.3 V
- 2 MHz Free-running Switching Frequency
- $\pm 2$  % Output Voltage Accuracy
- NCV Prefix for Automotive Requiring Site and Control Changes
- These Devices are Pb-Free and are RoHS Compliant

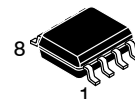
### Typical Applications

- Audio
- Infotainment
- Instrumentation
- Safety-Vision Systems



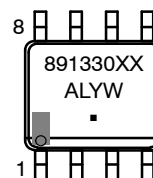
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**SOIC-8  
EXPOSED PAD  
CASE 751AC**

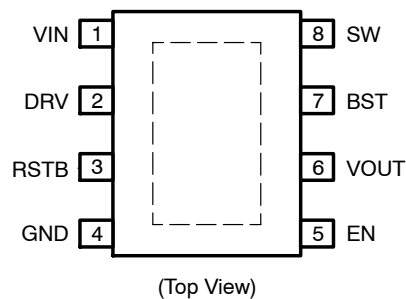
### MARKING DIAGRAM



With XX = 33 for 3.3 V Output  
38 for 3.8 V Output  
40 for 4.0 V Output  
50 for 5.0 V Output

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Device

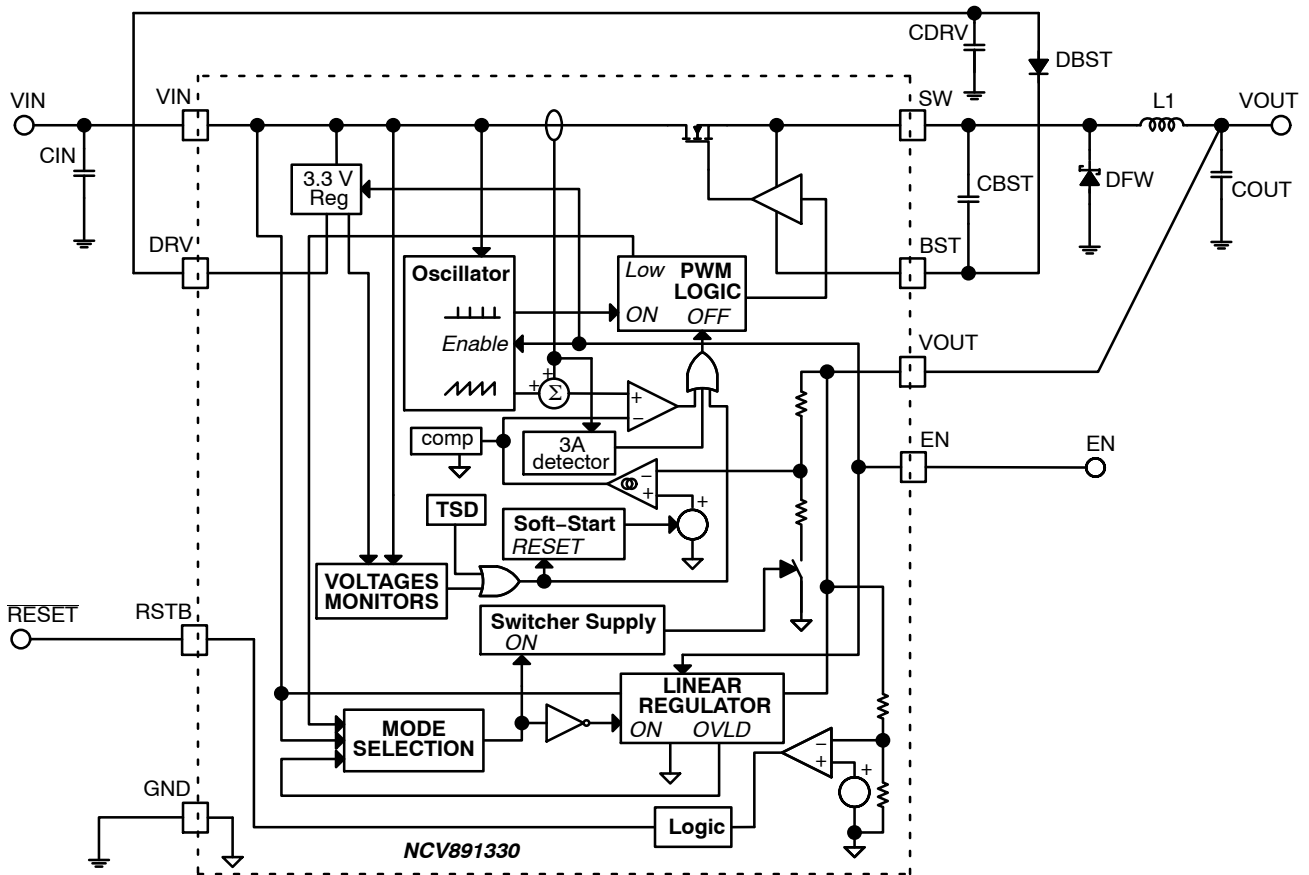
### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

# NCV891330



**Figure 2. Simplified Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

Pin No.	Pin Name	Description
1	VIN	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	DRV	Output voltage to provide a regulated voltage to the Power Switch gate driver.
3	RSTB	Reset function. Open drain output, pulling down to ground when the output voltage is out of regulation.
4	GND	Battery return, and output voltage ground reference.
5	EN	This TTL compatible Enable input allows the direct connection of Battery as the enable signal. Grounding this input stops switching and reduces quiescent current draw to a minimum.
6	VOUT	Output voltage feedback and LDO output. Feedback of output voltage used for regulation, as well as LDO output in LDO mode.
7	BST	Bootstrap input provides drive voltage higher than VIN to the N-channel Power Switch for minimum switch R <sub>ds(on)</sub> and highest efficiency.
8	SW	Switching node of the Regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
EPAD		Connect to Pin 4 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Min/Max Voltage VIN		-0.3 to 45	V
Max Voltage VIN to SW		45	V
Min/Max Voltage SW		-0.7 to 40	V
Min Voltage SW – 20 ns		-3.0	V
Min/Max Voltage EN		-0.3 to 40	V
Min/Max Voltage BST		-0.3 to 43	V
Min/Max Voltage BST to SW		-0.3 to 3.6	V
Min/Max Voltage on RSTB		-0.3 to 6	V
Min/Max Voltage VOUT		-0.3 to 18	V
Min/Max Voltage DRV		-0.3 to 3.6	V
Thermal Resistance, SOIC8-EP Junction-to-Ambient (Note 1)	R <sub>θJA</sub>	30	°C/W
Storage Temperature range		-55 to +150	°C
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +150	°C
ESD withstand Voltage (Note 2)	Human Body Model VESD	2.0	kV
Moisture Sensitivity	MSL	Level 2	
Peak Reflow Soldering Temperature (Note 3)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Value based on 4 layers of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness on FR4 PCB substrate.
- This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
- For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM/D

**Table 3. ELECTRICAL CHARACTERISTICS**

V<sub>IN</sub> = 4.5 to 28 V, V<sub>EN</sub> = 5 V, V<sub>BST</sub> = V<sub>SW</sub> + 3 V, C<sub>DRV</sub> = 0.1 μF, for typical values T<sub>J</sub> = 25°C, Min/Max values are valid for the temperature range -40°C ≤ T<sub>J</sub> ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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**QUIESCENT CURRENT**

Quiescent Current, enabled	V <sub>IN</sub> = 13.2 V, I <sub>OUT</sub> = 100 μA, 25°C	I <sub>q</sub>		30	39	μA
Quiescent Current, shutdown	V <sub>IN</sub> = 13.2 V, V <sub>EN</sub> = 0 V, 25°C	I <sub>qSD</sub>		9	12	μA

**UNDERVOLTAGE LOCKOUT – VIN (UVLO)**

UVLO Start Threshold	V <sub>IN</sub> rising	V <sub>UVLSTT</sub>	4.1		4.5	V
UVLO Stop Threshold	V <sub>IN</sub> falling	V <sub>UVLSTP</sub>	3.1		3.7	V
UVLO Hysteresis		V <sub>UVLOHY</sub>	0.4		1.4	V

**SOFT-START (SS)**

Soft-Start Completion Time		t <sub>SS</sub>	0.8	1.4	2.0	ms
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**OUTPUT VOLTAGE**

Output Voltage during regulation	100 μA < I <sub>OUT</sub> < 2.5 A 5.0 V option 4.0 V option 3.8 V option 3.3 V option	V <sub>OUTReg</sub>	4.9 3.92 3.724 3.234	5.0 4.0 3.8 3.3	5.1 4.08 3.876 3.366	V
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**OSCILLATOR**

Frequency	4.5 < V <sub>IN</sub> < 18 V 20 V < V <sub>IN</sub> < 28 V	F <sub>SW</sub> F <sub>SW(HV)</sub>	1.8 0.9	2.0 1.0	2.2 1.1	MHz
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- Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T<sub>J</sub> = T<sub>A</sub> = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

**Table 3. ELECTRICAL CHARACTERISTICS**

$V_{IN} = 4.5$  to  $28$  V,  $V_{EN} = 5$  V,  $V_{BST} = V_{SW} + 3$  V,  $C_{DRV} = 0.1$   $\mu$ F, for typical values  $T_J = 25^\circ\text{C}$ , Min/Max values are valid for the temperature range  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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**VIN FREQUENCY FOLDBACK MONITOR**

Frequency Foldback Threshold $V_{IN}$ rising $V_{IN}$ falling		$V_{FLDUP}$ $V_{FLDDN}$	18.4 18		20 19.8	V
Frequency Foldback Hysteresis		$V_{FLDHY}$	0.2	0.3	0.4	V

**MODE TRANSITION**

Normal to Low- $I_q$ mode Current Threshold	$8\text{ V} < V_{IN} < 28\text{ V}$	$I_{NtoL}$	3		40	mA
Mode Transition Duration Switcher to Linear Linear to Switcher		$t_{SWtoLIN}$ $t_{LINtoSW}$		300 1	2	$\mu$ s
Minimum time in Normal Mode before starting to monitor output current		$t_{SWblank}$		500		$\mu$ s
Linear to switcher transition at high $V_{in}$ at low $V_{in}$	$V_{OUT} = 3.3\text{ V}$	$V_{LINtoSW(HV)}$ $V_{LINtoSW(LV)}$	19 3.6		28 4.5	V

**PEAK CURRENT LIMIT**

Current Limit Threshold		$I_{LIM}$	3.9	4.4	4.9	A
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**POWER SWITCH**

ON Resistance	$V_{BST} = V_{SW} + 3.0\text{ V}$	$R_{DSON}$		180	360	$m\Omega$
Leakage current VIN to SW	$V_{SW} = 0, -40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	$I_{LKSW}$			10	$\mu$ A
Minimum ON Time	Measured at SW pin	$t_{ONMIN}$	45		70	ns
Minimum OFF Time	Measured at SW pin At $F_{SW} = 2\text{ MHz}$ (normal) At $F_{SW} = 500\text{ kHz}$ (max duty cycle)	$t_{OFFMIN}$	30	30 50	70	ns

**SLOPE COMPENSATION**

Ramp Slope (With respect to switch current)	$4.5 < V_{IN} < 18\text{ V}$ $20\text{ V} < V_{IN} < 28\text{ V}$	$S_{ramp}$ $S_{ramp(HV)}$	1.45 0.65	2.0 1.0	2.8 1.3	A/ $\mu$ s
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**LOW POWER LINEAR REGULATOR**

Line Regulation	$I_{OUT} = 5\text{ mA}, 6\text{ V} < V_{IN} < 18\text{ V}$	$V_{REG(line)}$		5	25	mV
Load Regulation	$V_{IN} = 13.2\text{ V}, 0.1\text{ mA} < I_{OUT} < 50\text{ mA}$	$V_{REG(load)}$		5	35	mV
Power Supply Rejection	$V_{OUT(ripple)} = 0.5\text{ V}_{p-p}, F = 100\text{ Hz}$	PSRR		65		dB
Current Limit		$I_{LIN(lim)}$	50		80	mA
Output clamp current	$V_{OUT} = V_{OUTreg(typ)} + 10\%$	$I_{CL(OUT)}$	0.5	1.0	1.5	mA

**SHORT CIRCUIT DETECTOR**

Switching frequency in short-circuit condition Analog Foldback Analog foldback – high $V_{IN}$ Hiccup Mode	$V_{OUT} = 0\text{ V}, 4.5\text{ V} < V_{IN} < 18\text{ V}$ $V_{OUT} = 0\text{ V}, 20\text{ V} < V_{IN} < 28\text{ V}$	$F_{SWAF}$ $F_{SWAFHV}$ $F_{SWHIC}$	450 225 24	550 275 32	650 325 40	kHz
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**RESET**

Leakage current into RSTB pin		$I_{RSTBIK}$			1	$\mu$ A
Output voltage threshold at which the RSTB signal goes low	$V_{OUT}$ decreasing 5.0 V option 4.0 V option 3.8 V option 3.3 V option	$V_{RESET}$	4.50 3.6 3.42 2.97	4.625 3.7 3.515 3.05	4.75 3.8 3.61 3.14	V

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

**Table 3. ELECTRICAL CHARACTERISTICS**

$V_{IN} = 4.5$  to  $28$  V,  $V_{EN} = 5$  V,  $V_{BST} = V_{SW} + 3$  V,  $C_{DRV} = 0.1$   $\mu$ F, for typical values  $T_J = 25^\circ\text{C}$ , Min/Max values are valid for the temperature range  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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**RESET**

Hysteresis on RSTB threshold	$V_{OUT}$ increasing 5.0 V option 4.0 V option 3.8 V option 3.3 V option	$V_{RESHys}$	25 20 19 17	60 50 45 40	100 80 76 66	mV
Noise-filtering delay	From $V_{OUT} < V_{RESET}$ to RSTB pin going low	$t_{filter}$	10		25	$\mu$ s
Restart Delay time	From $V_{OUT} > V_{RESET} + V_{RESHys}$ to high RSTB	$t_{delay}$	14	16	18	ms
Low RSTB voltage	$R_{RSTBpullup} = V_{OUTreg}/1$ mA, $V_{OUT} > 1$ V	$V_{RSTBlow}$			0.4	V

**GATE VOLTAGE SUPPLY (DRV pin)**

Output Voltage		$V_{DRV}$	3.1	3.3	3.5	V
DRV UVLO START Threshold		$V_{DRVSTT}$	2.7	2.9	3.05	V
DRV UVLO STOP Threshold		$V_{DRVSTP}$	2.5	2.8	3.0	V
DRV UVLO Hysteresis		$V_{DRVHYS}$	50		200	mV
DRV Current Limit	$V_{DRV} = 0$ V	$I_{DRVLIM}$	21		50	mA

**VIN OVERVOLTAGE SHUTDOWN MONITOR**

Overvoltage Stop Threshold	$V_{IN}$ increasing	$V_{OVSTP}$	36.5	37.7	39.0	V
Overvoltage Start Threshold	$V_{IN}$ decreasing	$V_{OVSTT}$	36.0	37.3	38.8	V
Overvoltage Hysteresis		$V_{OVHY}$	0.25	0.40	0.50	V

**ENABLE (EN)**

Logic low threshold voltage		$V_{ENlow}$	0.8			V
Logic high threshold voltage		$V_{ENhigh}$			2	V
EN pin input current		$I_{ENbias}$	0.2		1	$\mu$ A

**THERMAL SHUTDOWN**

Activation Temperature		TSD	155		190	$^\circ\text{C}$
Reset temperature		$TSD_{restart}$	135		185	$^\circ\text{C}$
Hysteresis		$T_{HYS}$	5		20	$^\circ\text{C}$

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

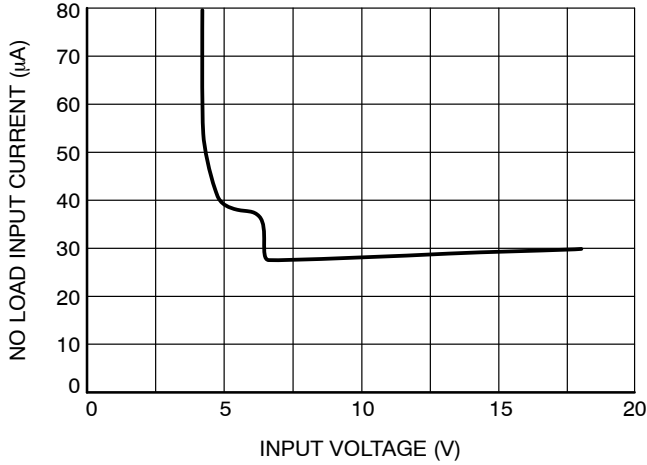


Figure 3. No-load Input Current at  $T_J = 25^{\circ}\text{C}$  vs. Input Voltage

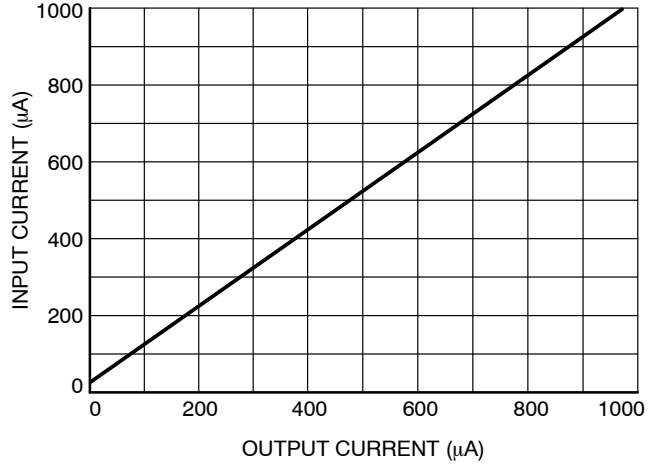


Figure 4. Input Current at  $T_J = 25^{\circ}\text{C}$  vs. Output Current

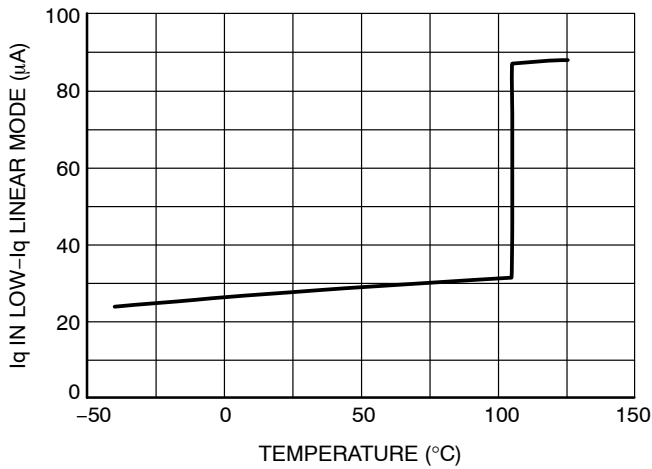


Figure 5. Low- $I_q$  Mode Quiescent Current vs. Junction Temperature

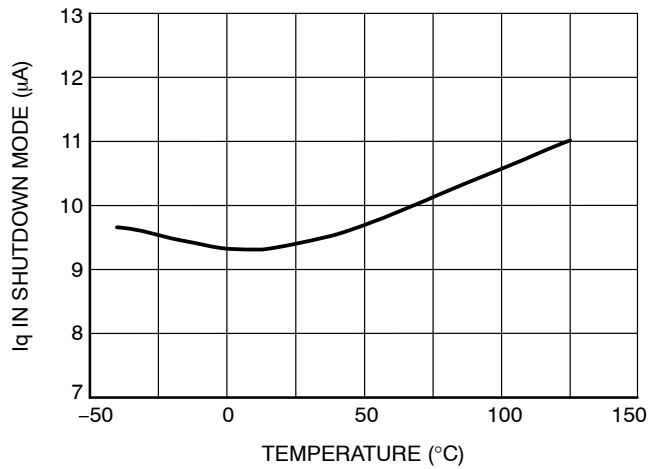


Figure 6. Shutdown Mode Quiescent Current vs. Junction Temperature

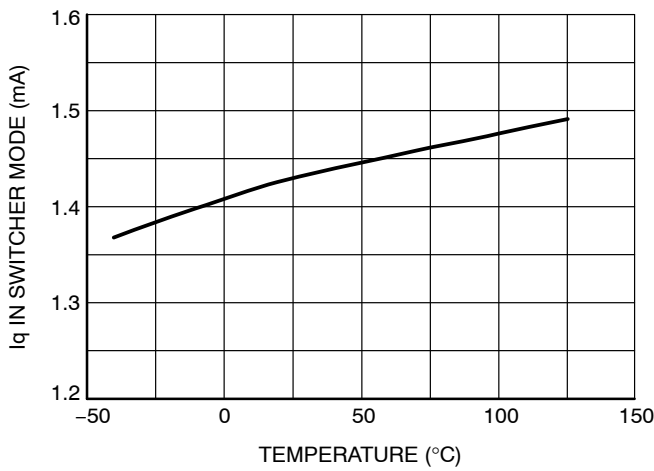


Figure 7. Switching Mode Quiescent Current vs. Junction Temperature

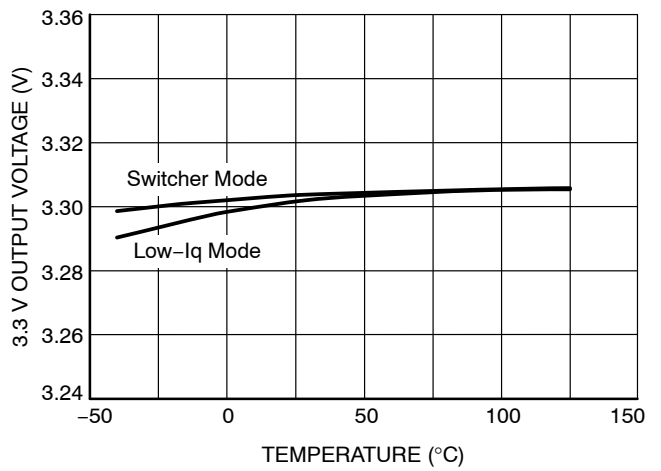


Figure 8. 3.3 V Output Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

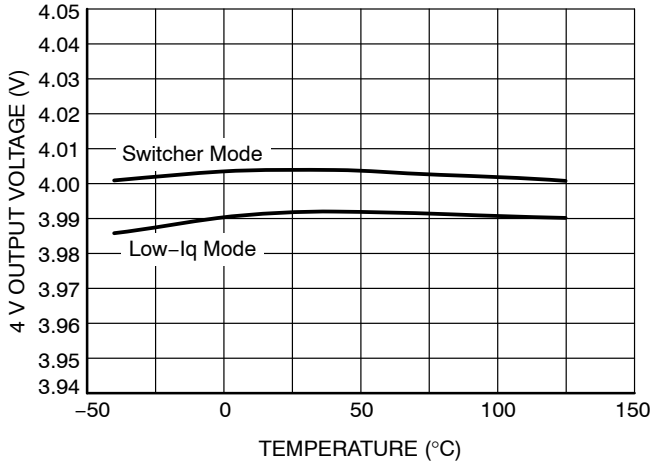


Figure 9. 4.0 V Output Voltage vs. Junction Temperature

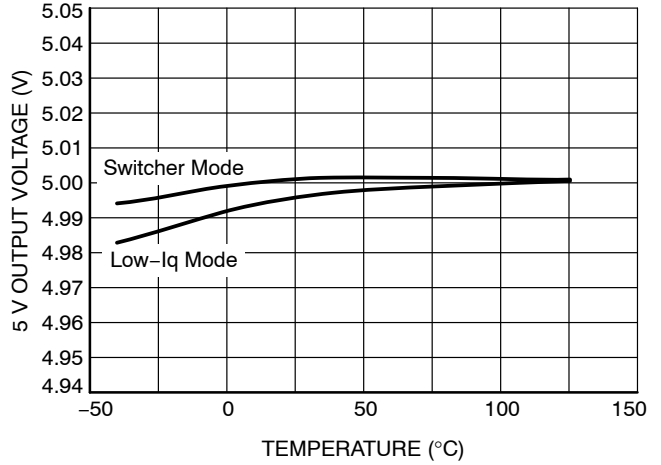


Figure 10. 5.0 V Output Voltage vs. Junction Temperature

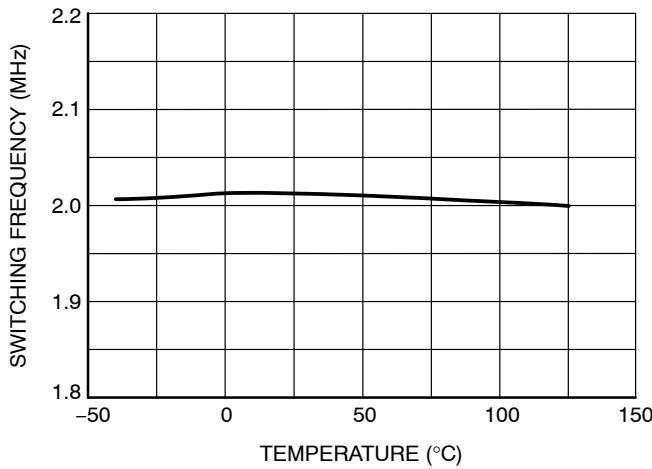


Figure 11. Switching Frequency vs. Junction Temperature

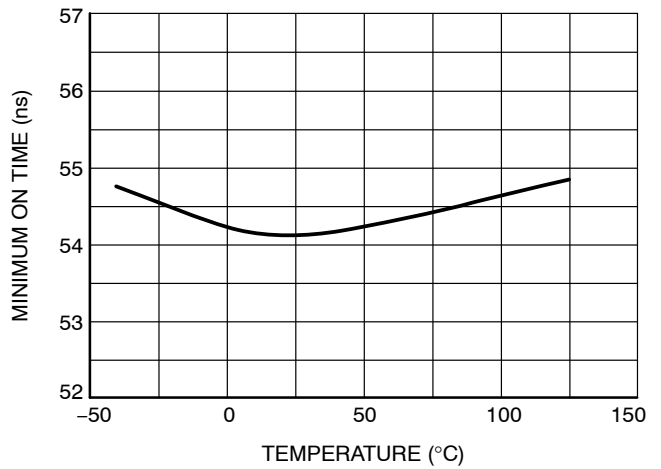


Figure 12. Minimum On Time vs. Junction Temperature

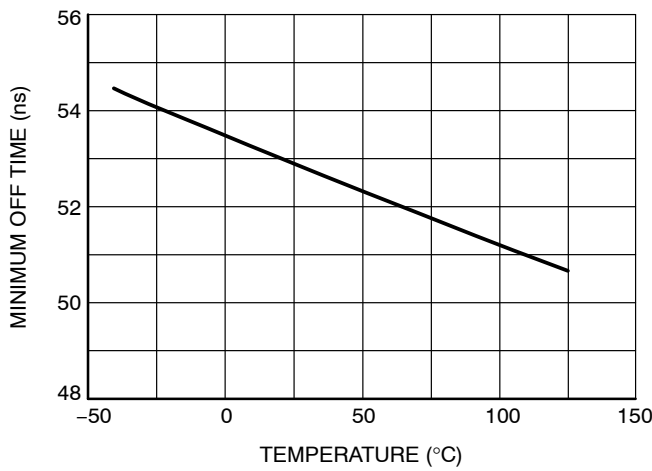


Figure 13. Minimum Off Time vs. Junction Temperature

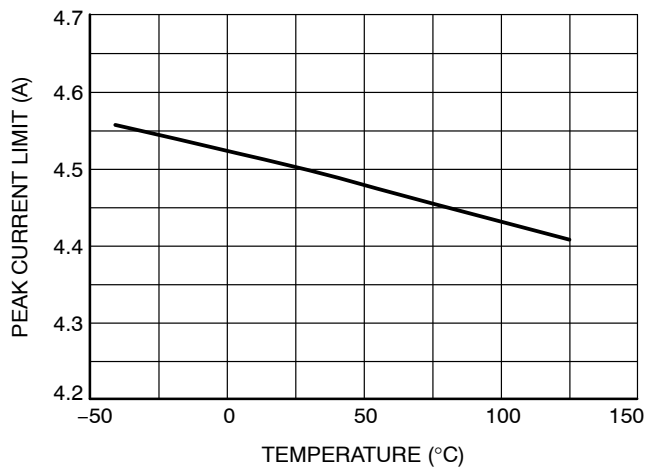


Figure 14. Peak Current Limit vs. Junction Temperature

TYPICAL CHARACTERISTICS

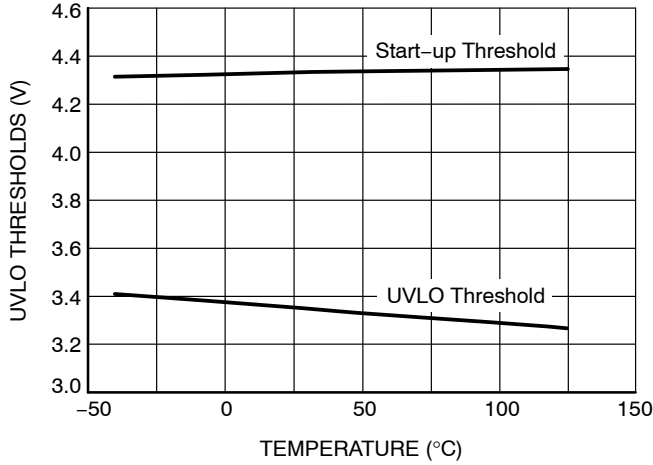


Figure 15. UVLO Thresholds vs. Junction Temperature

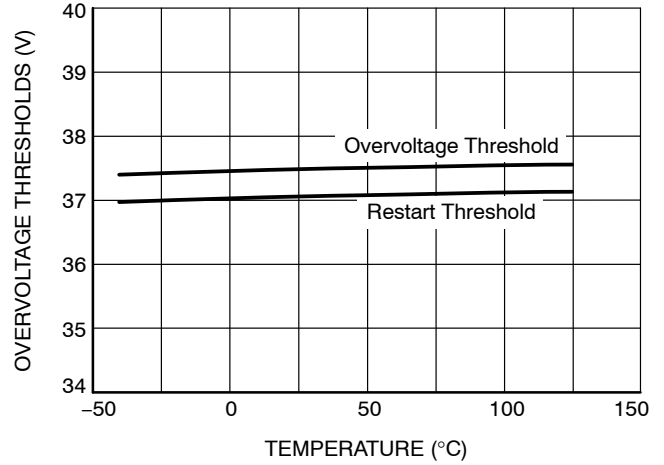


Figure 16. Input Overvoltage Thresholds vs. Junction Temperature

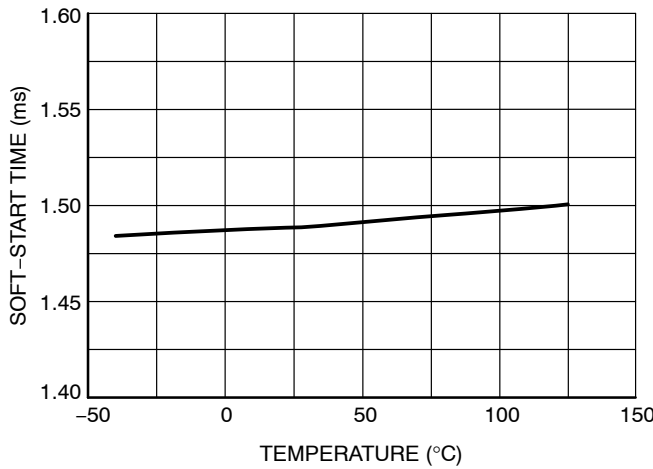


Figure 17. Soft-start Duration vs. Junction Temperature

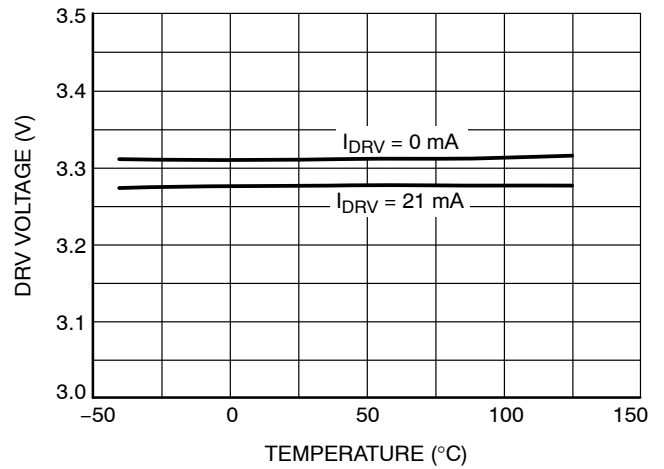


Figure 18. DRV Voltage vs. Junction Temperature

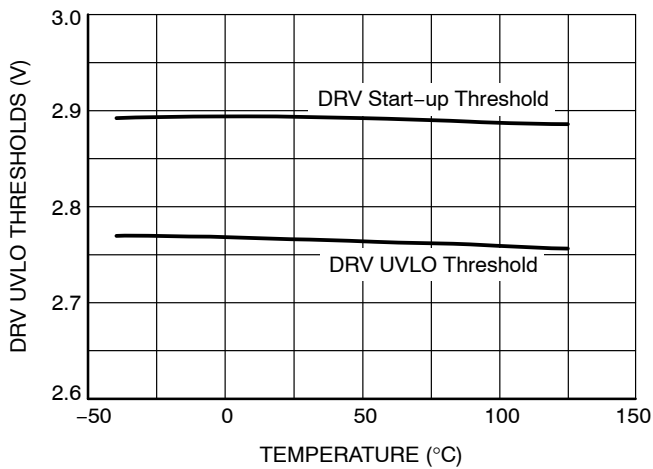


Figure 19. DRV Voltage UVLO Thresholds vs. Junction Temperature

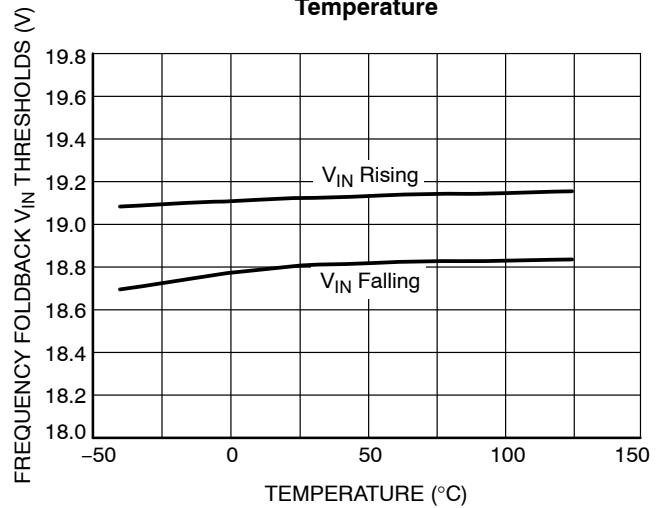


Figure 20. Frequency Foldback Voltage Thresholds vs. Junction Temperature



TYPICAL CHARACTERISTICS

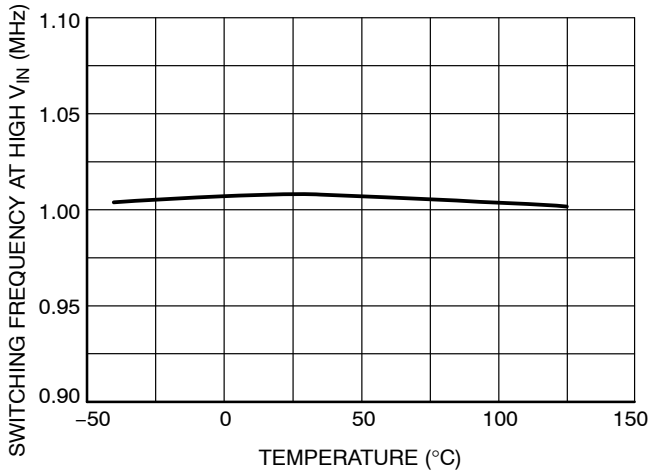


Figure 21. Foldback Frequency vs. Junction Temperature

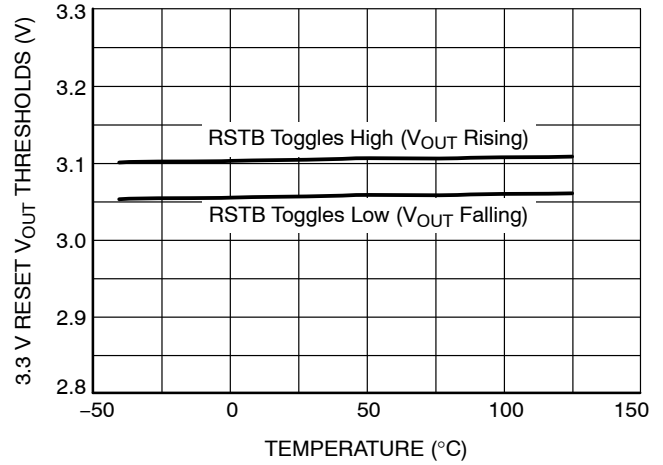


Figure 22. 3.3 V Version RESET Thresholds vs. Junction Temperature

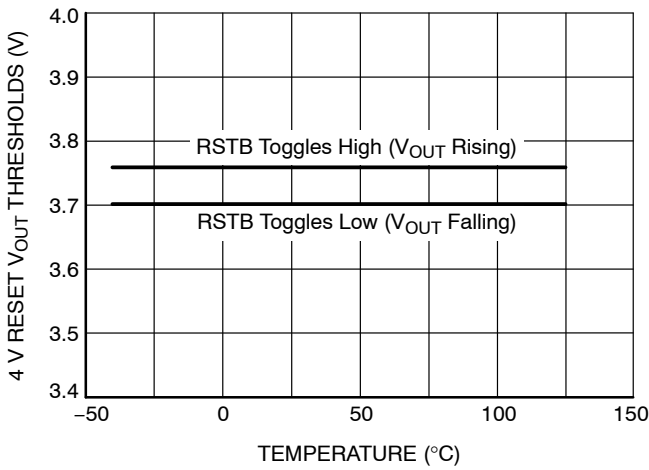


Figure 23. 4.0 V Version RESET Thresholds vs. Junction Temperature

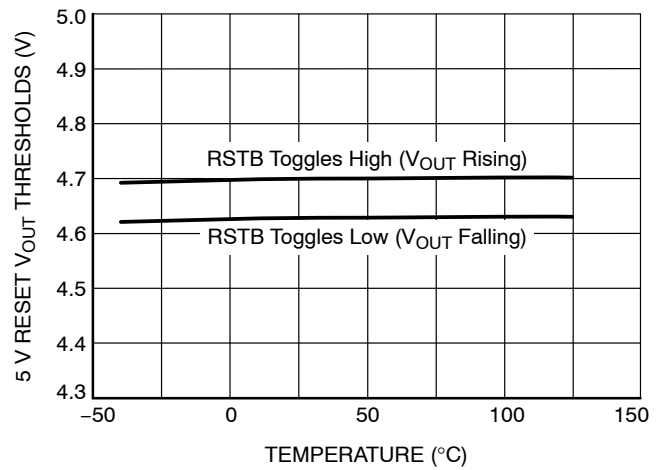


Figure 24. 5.0 V Version RESET Thresholds vs. Junction Temperature

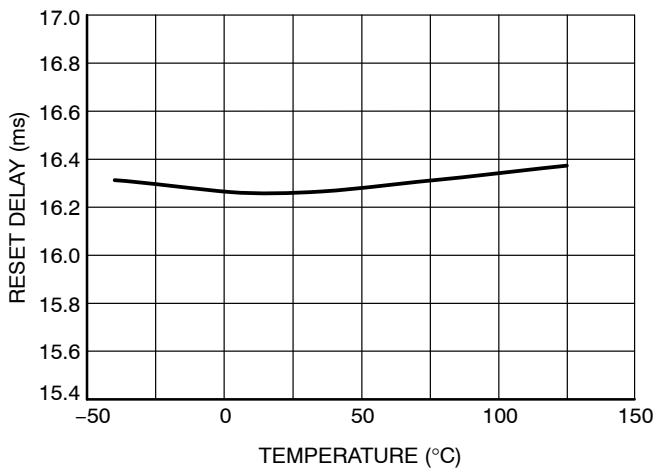


Figure 25. RESET Delay vs. Junction Temperature

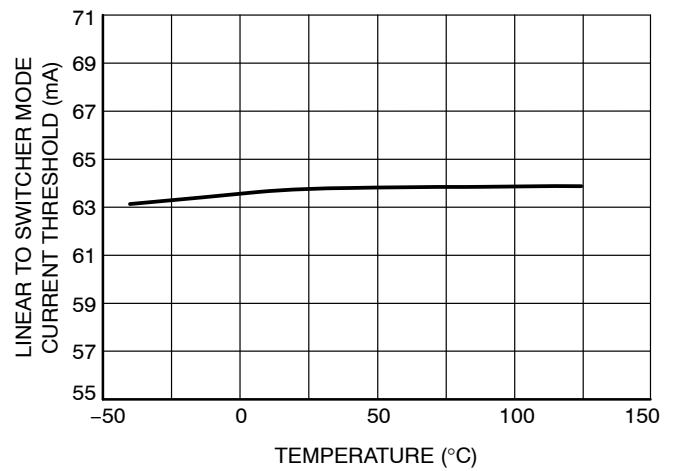


Figure 26. Low-I<sub>q</sub> to Switcher Mode Transition vs. Junction Temperature

TYPICAL CHARACTERISTICS

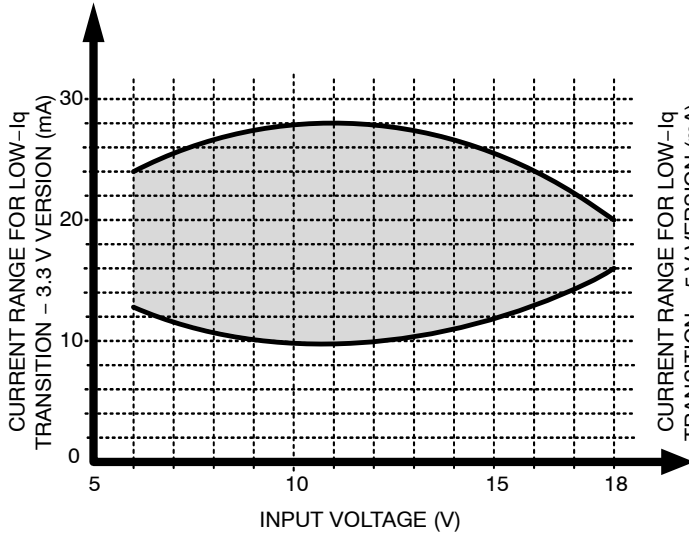


Figure 27. Switcher to Low-Iq Mode Transition (3.3 V Version, 2.2  $\mu$ H) vs. Input Voltage

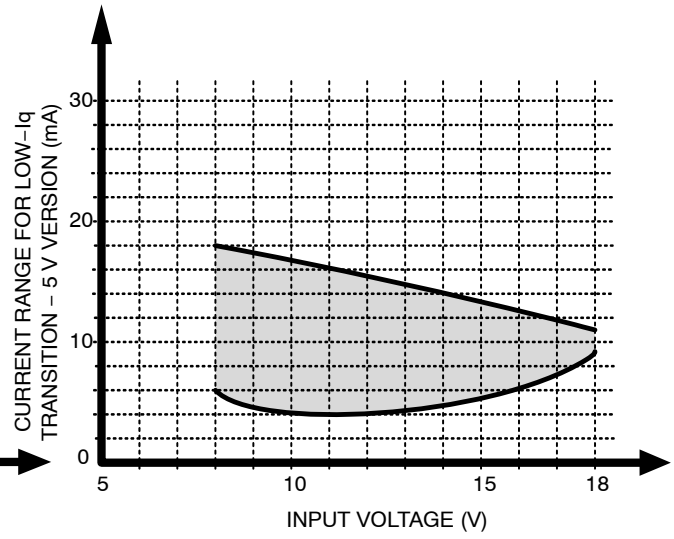


Figure 28. Switcher to Low-Iq Mode Transition (5.0 V Version, 2.2  $\mu$ H) vs. Input Voltage

APPLICATION INFORMATION

Hybrid Low-Power Mode

A high-frequency switch-mode regulator is not very efficient in light load conditions, making it difficult to achieve low-Iq requirements for sleep-mode operation. To remedy this, the NCV891330 includes a low-Iq linear regulator that turns on at light load, while the PWM regulator turns off, ensuring a high-efficiency low-power operation. Another advantage of linear mode is the tight regulation free of voltage ripple usually associated with low-Iq switchers in light load conditions.

At initial start-up the NCV891330 always runs in PWM converter mode, regardless of the output current, and goes through a soft start. It then stays in PWM mode if the output current is high enough. If the output current is low, the NCV891330 transitions to Linear Regulator mode, after a 300 μs period during which it assesses the level of output current. Note that the Reset signal needs to be high before the IC starts to look at the output current level.

It stays in this low-power mode until the output current exceeds the  $I_{LIN(lim)}$  limit: it then transitions to PWM

converter mode. This transition happens in less than 2 μs, so that the transient response is not affected by the mode change.

Once the NCV891330 has transitioned to switcher mode, it cannot go back to low-Iq mode before a 500 μs blanking period has elapsed, after which it starts looking at the output current level.

If the NCV891330 is in low-Iq Linear Regulator mode in normal battery range, it will transition to switcher mode when  $V_{IN}$  increases above  $V_{LINToSW(HV)}$ , regardless of the output current. Similarly, if the NCV891330 is in PWM mode and  $V_{IN}$  is higher than  $V_{FLDUB}$ , it will not transition to low-Iq Linear mode even if the output current becomes lower than  $I_{NtoL}$ .

At low input voltage, the NCV891330 stays in low-Iq mode down to  $V_{LINToSW(LV)}$  if it entered this mode while in normal battery range. However it may not enter low-Iq mode below 8 V depending on the charge of the bootstrap capacitor (see Bootstrap section and typical characteristics curves for details).

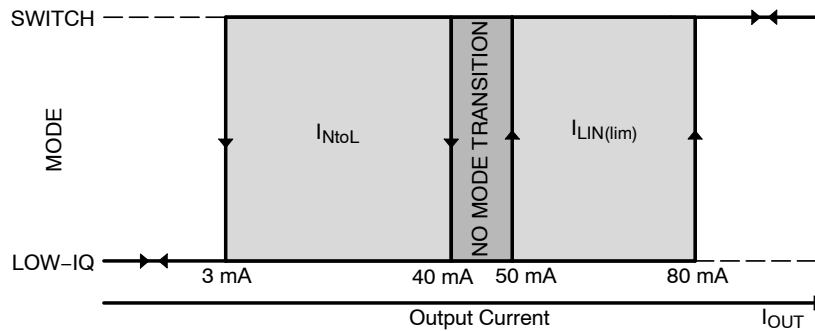


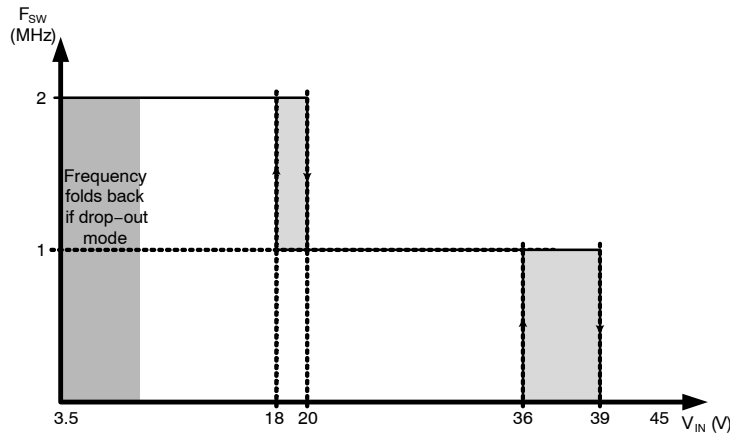
Figure 29. Mode Transition Diagram for Input Voltages between 8.0 V and  $V_{LINToSW(HV)}$

**Input Voltage**

An Undervoltage Lockout (UVLO) circuit monitors the input. The circuit can inhibit switching and reset the Soft-start circuit if there is insufficient voltage for proper regulation. Depending on the output conditions (voltage option and loading), the NCV891330 may lose regulation and run in drop-out mode before reaching the UVLO threshold: refer to the Minimum Vin calculation tool for details. When the input voltage drops low enough that the part cannot regulate because it reaches its maximum duty cycle, the switching frequency is divided down by up to 4 (down to 500 kHz). This helps lowering the minimum voltage at which the regulator loses regulation.

An overvoltage monitoring circuit automatically terminates switching if the input voltage exceeds  $V_{OVSTP}$  (see Figure 30), but the NCV891330 can withstand input voltages up to 45 V.

To avoid skipping switching pulses and entering an uncontrolled mode of operation, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the  $V_{IN}$  Frequency Foldback threshold (see Figure 30). Frequency reduction is automatically terminated when the input voltage drops back below the  $V_{IN}$  Frequency Foldback threshold. This also helps to limit the power lost in switching and generating the drive voltage for the Power Switch.



**Figure 30. NCV891330 Switching Frequency Profile vs. Input Voltage**

**Soft-Start**

Upon being enabled or released from a fault condition, and after the DRV voltage is established, a soft-start circuit ramps the switching regulator error amplifier reference voltage to the final value. During soft-start, the average switching frequency is lower until the output voltage approaches regulation.

**Slope Compensation**

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope

compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub-harmonic oscillations. The recommended inductor values are 2.2 or 3.3  $\mu$ H, although higher values are possible.

**Current Limiting**

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 31 shows – for a 2.2  $\mu$ H inductor – how the variation of inductor peak current with input voltage affects the maximum DC current the NCV891330 can deliver to a load.

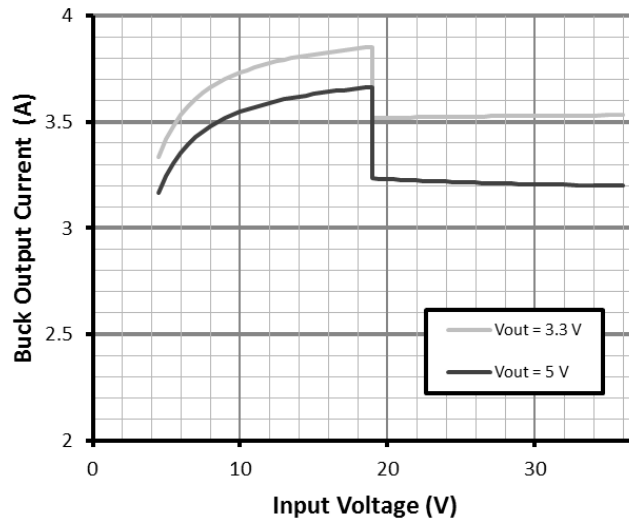


Figure 31. NCV891330 Load Current Capability with a 2.2  $\mu$ H Inductor

**Short Circuit Protection**

During severe output overloads or short circuits, the NCV891330 automatically reduces its switching frequency. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed.

In more severe short-circuit conditions where the inductor current is still too high after the switching frequency has fully folded back, the regulator enters a hiccup mode that further reduces the power dissipation and protects the system.

**RESET Function**

The RSTB pin is pulled low when the output voltage falls below 7.5% of the nominal regulation level, and floats when the output is properly regulated. A pull-up resistor tied to the output is needed to generate a logic high signal on this open drain pin. The pin can be left unconnected when not used.

When the output voltage drops out of regulation, the pin goes low after a short noise-filtering delay ( $t_{filter}$ ). It stays low for a 16 ms delay time after the output goes back to regulation, simplifying the connection to a micro-controller.

The RSTB pin is also pulled low immediately in case of VIN overvoltage, Thermal shutdown, VIN UVLO or DRV UVLO.

**Feedback Loop**

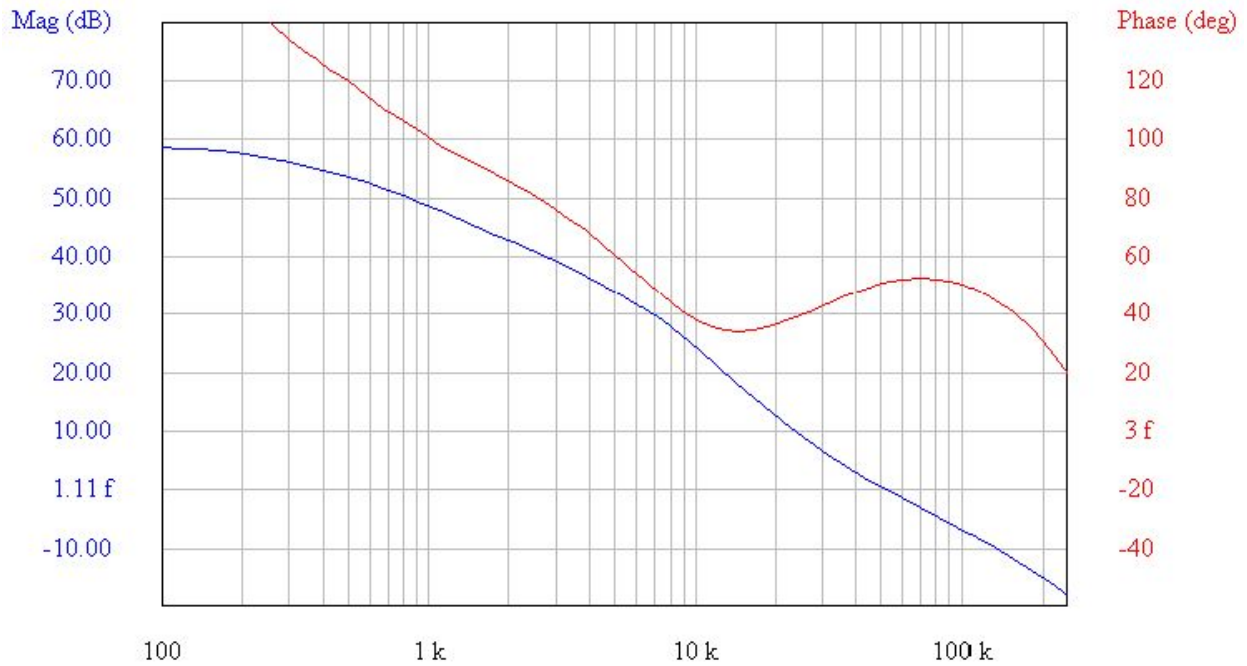
All components of the feedback loop (output voltage sensing, error amplifier and compensation) are integrated inside the NCV891330, and are optimized to ensure regulation and sufficient phase and gain margin for the recommended conditions of operation.

Recommended conditions and components:

- Input: car battery
- Output: 3.3 V, 3.8 V, 4 V or 5 V, with output current up to 3 A
- Output capacitor: 30  $\mu$ F capacitance
- Inductor: 2.2  $\mu$ H to 3.3  $\mu$ H

With these operating conditions and components, the open loop transfer function has a phase margin greater than 50°, as can be seen in Figure 32.

## NCV891330



**Figure 32. Bode Plot of the Open Loop Transfer Function of a Buck Converter using the NCV891330 for  $V_{in} = 13\text{ V}$ ,  $V_{out} = 3.3\text{ V}$ ,  $I_{out} = 2\text{ A}$ ,  $C_{out} = 3 \times 10\text{ }\mu\text{F}$  and  $L = 2.2\text{ }\mu\text{H}$**

For more details and for effect of component values other than the recommended ones, please refer to the design spreadsheet provided on the [www.onsemi.com](http://www.onsemi.com) NCV891330 page.

The design spreadsheet also includes the total open loop transfer function for the output voltage sensing at the NCV891330 VOUT pin to the output voltage.

**Bootstrap**

At the DRV pin an internal regulator provides a ground-referenced voltage to an external capacitor ( $C_{DRV}$ ), to allow fast recharge of the external bootstrap capacitor ( $C_{BST}$ ) used to supply power to the power switch gate driver. If the voltage at the DRV pin goes below the DRV UVLO Threshold  $V_{DRVSTB}$  switching is inhibited and the Soft-start circuit is reset, until the DRV pin voltage goes back up above  $V_{DRVSTT}$ .

The NCV891330 permanently monitors the bootstrap capacitor, and always ensures it stays charged no matter what the operating conditions are. As a result, the additional charging current for the bootstrap capacitor may prevent the regulator from entering Low-Iq mode at low input voltage. Practically, the 5 V output version does not enter Low-Iq mode for input voltages below 8 V, and the 3.8 V and 4 V versions for input voltages below 6.5 V (see typical characteristics curves for details).

**Enable**

The NCV891330 is designed to accept either a logic level signal or battery voltage as an Enable signal. However if

voltages above 40 V are expected, EN should be tied to VIN through a 10 k $\Omega$  resistor in order to limit the current flowing into the overvoltage protection of the pin.

EN low induces a shutdown mode which shuts off the regulator and minimizes its supply current to 9  $\mu$ A typical by disabling all functions.

Upon enabling, voltage is established at the DRV pin, followed by a soft-start of the switching regulator output.

**Thermal Shutdown**

A thermal shutdown circuit inhibits switching, resets the Soft-start circuit, and removes DRV voltage if internal temperature exceeds a safe level. Switching is automatically restored when temperature returns to a safe level.

**Exposed Pad**

The exposed pad (EPAD) on the back of the package must be electrically connected to the electrical ground (GND pin) for proper, noise-free operation.

**ORDERING INFORMATION**

Device	Output	Package	Shipping
NCV891330PD50R2G	5.0 V	SOIC-8 EP (Pb-Free)	2500 / Tape & Reel
NCV891330PD40R2G	4.0 V		
NCV891330PD38R2G	3.8 V		
NCV891330PD33R2G	3.3 V		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



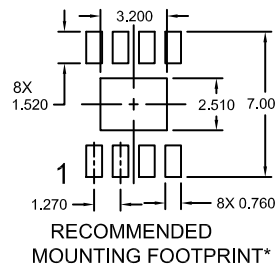
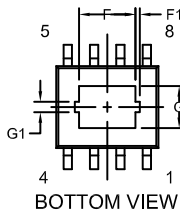
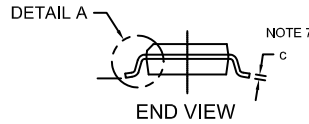
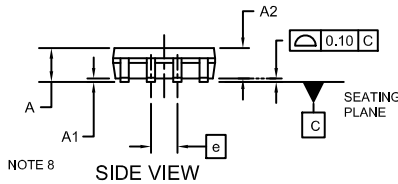
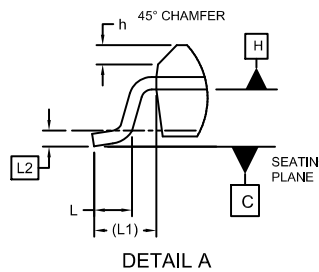
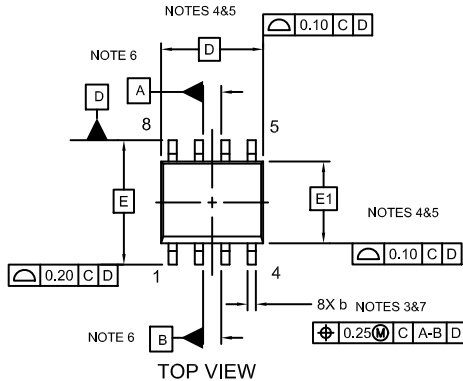
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## SOIC-8 EP CASE 751AC ISSUE D

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NOTES:

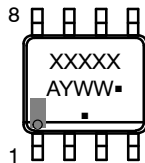
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
∅	0°	4°	8°

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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